Output Gain Stage - Current Output Configuration (Group 2 only)

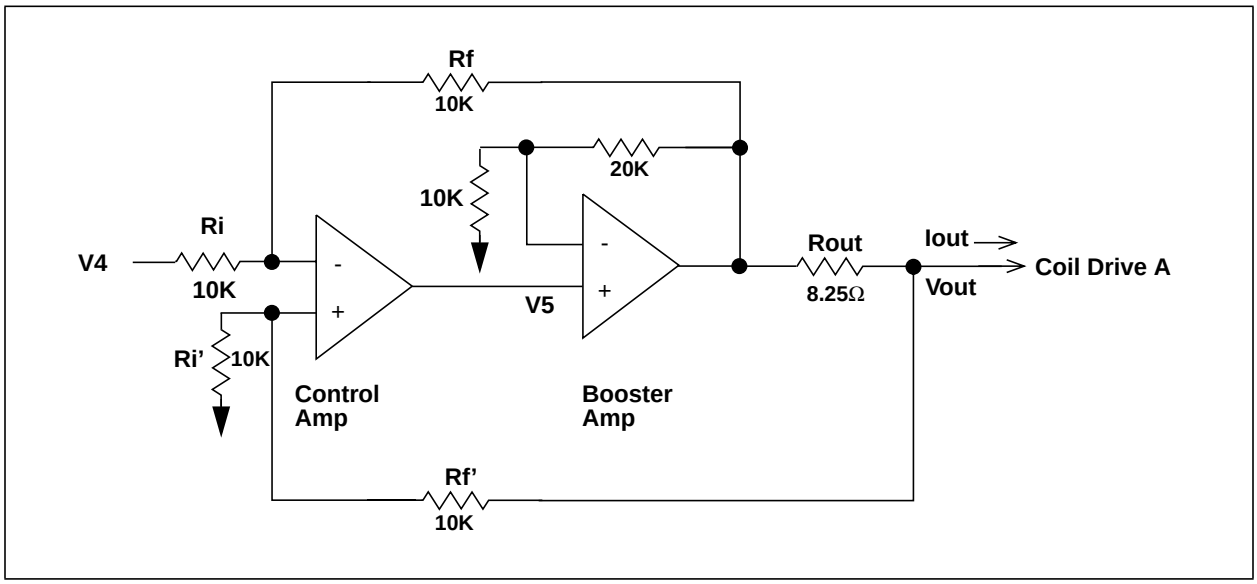


Figure 3-121. QCA Output Gain Stage - Group 2

The following closed loop gain equation applies to the output stage of Group 2 boards illustrated in Figure 3-121:

Iout = -(V4/Rout)*(Rf/Ri) = -V4/Rout

Ri = closely matched input resistors

Rf = closely matched feedback resistors

Rout = 8.25 ohms

Channel Configuration Examples

Unipolar Voltage In - Unipolar Voltage Out (Group 1)

This section contains calculations for selecting resistors for the following channel specifications:

- Input Voltage: 0 to -10V
- Output Voltage: 0 to 12.5V
- Load Resistance: 50 ohms

1. Enable the invert jumper (shown in Figure 3-122) since the input voltage sign is opposite from the output voltage sign.

2. Since the magnitude of the input must be gained up to get the full output voltage range, the output gain stage will need a gain greater than 1. Set the output gain stage to a gain of 2. This means Rf-B is 10KΩ (see Figure 3-120).

3. Referring to Figure 3-120:

   $V_{out\ MAX} = 12.5V$
   $V_{out,\ booster\ amp\ MAX} = 12.5V + (Rout)*(Iout) = 12.5V + (2\Omega)*(250mA) = 13V$

   which is less than the maximum 15V allowed.

4. If the output stage has a gain of 2, V4 in Figure 3-119 has the range: 0 to -6.25V. Assume no offset is needed (Offset jumper in DIS position), so the offset adjustment stage is a unity gain inverting stage which means V2 = 0 to 6.25V.

5. Since V2 = 0 to 6.25V and V1 = 0 to 10V (after the actuator position request has been inverted), V2 = 0.625*V1. This implies that:

   RB/(RA1 + RA2 + RB) = 0.625

   Let RA1 = 1k potentiometer, RA2 = 4.53K, and RB = 7.96k. By adjusting the 1k potentiometer, the ratio of resistors falls between 0.590 and 0.637 which includes the desired 0.625 ratio.

6. The offset adjustment stage may be used to add a small offset to the valve position request to make sure the output voltage is always positive. If a 10 to 50 mV offset is desired:

   RD/(RC1 + RC2 + RD) = 0.001 to 0.005

   Let RC1 = 50k potentiometer, RC2 = 9.76k, and RD = 50 ohms. By adjusting the 50k potentiometer, the ratio of resistors falls between 0.0008 and 0.0051. When multiplied by 10Vref, the desired 10 to 50mV offset is added to the signal.

Unipolar Voltage In - Unipolar Current Out (Group 2)

This section contains calculations for selecting resistors for the following channel specifications:

- Input Voltage: 0 to -10V
- Output Current: 0 to 250mA
- Load Resistance: 50Ω

1. Enable the invert jumper (shown in Figure 3-122) since the input voltage sign is opposite from the output current sign.

2. Referring to Figure 3-121:

Vout (booster amp MAX) = (Rload + Rout)*(Iout) = (50Ω + 8.25Ω) * 250mA = 14.56V which is less than the maximum 15V allowed.

The output stage has unity gain where Rf = Ri. Since Rout is 8.25 ohms and Iout = 0 to 250mA:

V4 = 0 to -2.06V

3. Assume no offset is needed (Offset jumper in DIS position), so the offset adjustment stage is a unity gain inverting stage which implies V2 = 0 to 2.06V.

4. Since V2 = 0 to 2.06V and V1 = 0 to 10V (after the valve position request has been inverted), V2 = 0.206*V1. This implies that:

RB/(RA1 + RA2 + RB) = 0.206

Let RA1 = 1K potentiometer, RA2 = 7.5K, and RB = 2K. By adjusting the 1K potentiometer, the ratio of resistors ranges between 0.190 and 0.267, which includes the desired 0.625 ratio.

Calibration

To calibrate a QCA card, adjust the range and offset potentiometers on the front card edge while the output voltage or current is monitored. Since channel output drives cannot be disconnected on power-up and potentiometer settings may be unknown initially, it is suggested that outputs be disconnected from the actuators initially. Instead, a resistor (approximately equal to coil load resistance) of sufficient power rating may be connected to the output at the halfshell on power-up, and the potentiometers may be adjusted to safe operating values.

Note

Group 2 boards which have true current outputs, should have a load on the output when powered up. If no load is present and V4 (see Figure 3-119) has a slight voltage present due to the input voltage or the offset voltage, the output will saturate because the channel is trying to drive a preset current into an infinite load.

The following calibration steps apply to unipolar voltage input to unipolar voltage or current output QCA boards. Steps are included to add in a small offset which keeps the output coil drive from crossing over the 0V or 0A boundary and switching polarities, if this is a necessary constraint.

1. Disable the offset jumper (see Figure 3-122).

2. Send the full scale actuator position request, and adjust the range potentiometer on the front card edge for the channel being calibrated until Vout (Group 1) or Iout (Group 2) equals the desired full scale output for the channel.

3. Send the bottom of scale actuator position request and check if Vout (Group 1) or Iout (Group 2) is at the desired bottom of scale. If the output is satisfactory, then calibration is done.

4. If offset is needed, enable the offset jumper and adjust the offset potentiometer until Vout (Group 1) or Iout (Group 2) is acceptable and return to Step 2.

3-16.6. Controls and Indicators

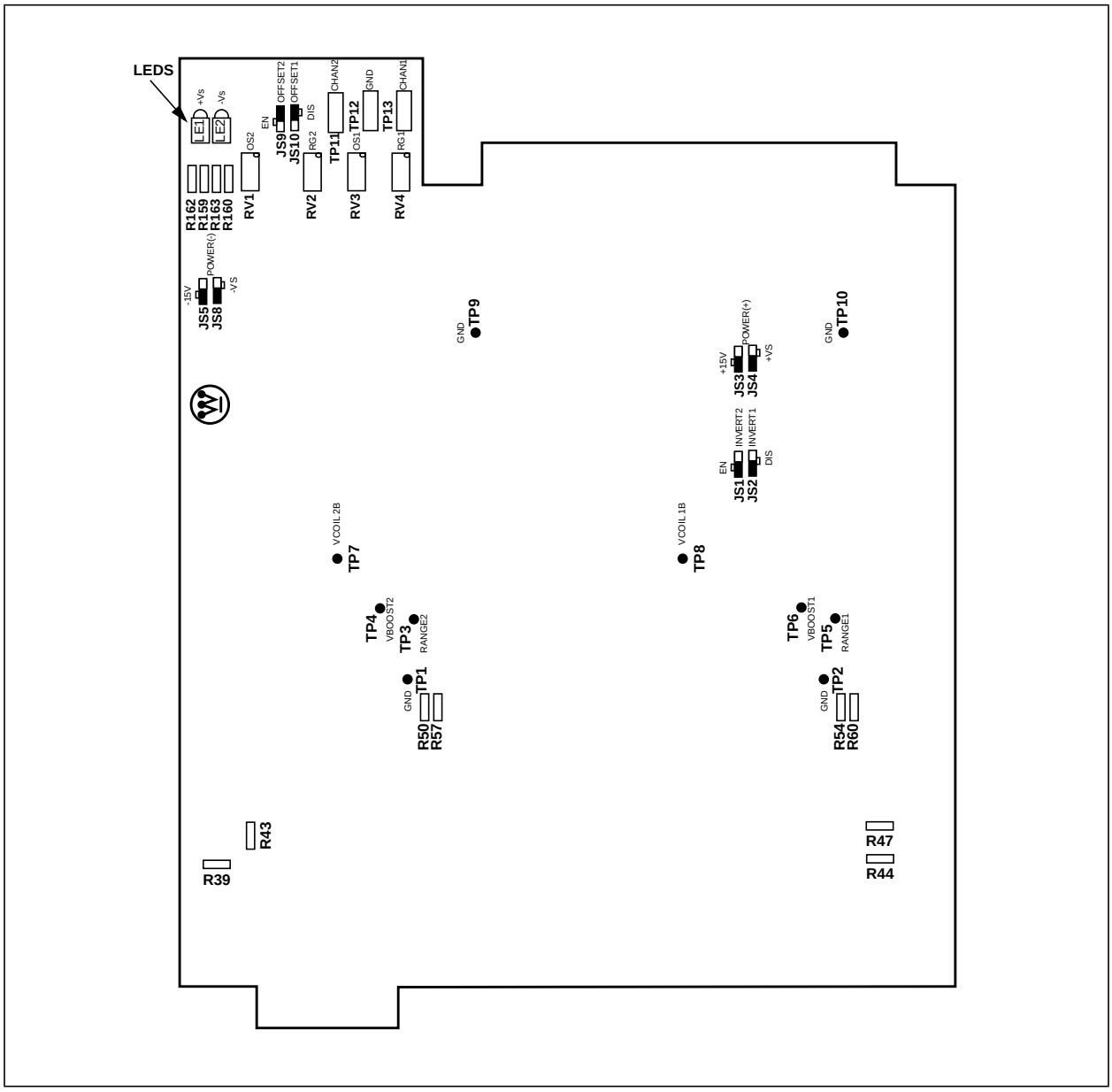


Figure 3-122. QCA Card Outline and User Controls

LED Indicators

+VS: lit when +21V on-board supply is alive

-VS: lit when -21V on-board supply is alive

Plug-in Resistors

Table 3-80. QCA Plug-in Scaling Resistor Reference Designators

Channel	Range Adjust Resistors	Offset Adjust Resistors	*Gain Adjust Resistors (Rf-B)
#1	RA2: R54 RB: R60	RC2: R160 RD: R163	DriveA - R44 DriveB - R47
#2	RA2: R50 RB: R57	RC2: R159 RD: R162	DriveA - R43 DriveB - R39
* Group 1 Only			

Potentiometers

Range Adjustment Potentiometer RA1: used to adjust the signal range of a channel during calibration.

Channel 1 - Reference Designator RV4; Label RG1

Channel 2 - Reference Designator RV2; Label RG2

Offset Adjustment Potentiometer RC1: used to adjust the signal offset of a channel during calibration.

Channel 1 - Reference Designator RV3; Label OS1

Channel 2 - Reference Designator RV1; Label OS2

Test Jacks

CHANx - test jack providing Vcoil Drive A output voltage of channel x to be monitored during calibration. (x = 1,2) Reference Designators: TP13 (channel 1), TP11 (channel 2)

GND - test jack providing signal ground. Reference Designator: TP12

Jumpers

POWER(+): Always set jumpers to +15V position.
DEFAULT Group 1 and 2: +15V position

POWER(-): Always set jumpers to -15V position.
DEFAULT Group 1 and 2: -15V position

OFFSET: If jumper set to EN (enable), offset is added to the channel's actuator position request. When set to DIS (disable), no offset is added. DEFAULT Group 1 and 2: DIS position

INVERT: If jumper is set to EN, the channel actuator position request is inverted in the input stage. DEFAULT Group 1 and 2: EN position

Table 3-81. Reference Designators for QCA Jumpers - Groups 1 and 2

Channel	Offset	Invert	*Power(+)	*Power(-)
#1	JS10	JS2	JS3 JS4	JS5 JS8
#2	JS9	JS1		
* Note: Power (+) and (-) jumpers are not channel specific				

Test Points

Test points appear at the output of those stages denoted by V2, V4, and Coil Drives in Figure 3-116. These test points plus the ground test points with their reference designators are listed in Table 3-82 for each channel.

Table 3-82. QCA Test Point Reference Designators

Channel	Range Adjust Stage Output	Offset Adjust Stage Output	Gain Adjust Stage Output	Ground
#1	TP5	TP6	DriveA: TP13 *DriveB: TP8	TP1, TP2, TP9, TP10, TP12
#2	TP3	TP4	DriveA: TP11 *DriveB: TP7	
* Group 1 Only				

3-16.7. Installation Data Sheets

1 of 3

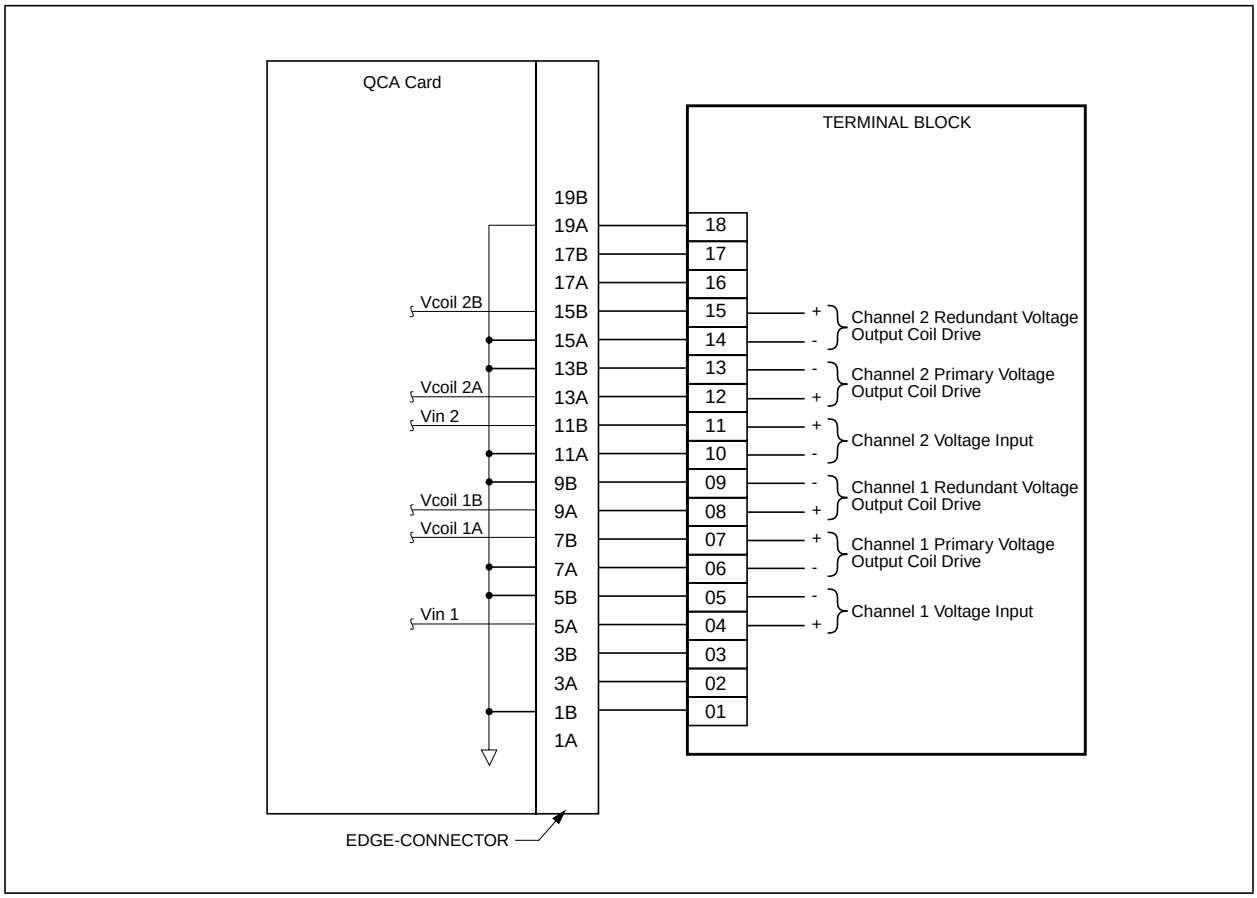


Figure 3-123. QCA Wiring Diagram (Group 1)
(Using AMP-18 conductor 18 AWG wiring) (3A99512)

Installation Data Sheet

2 of 3

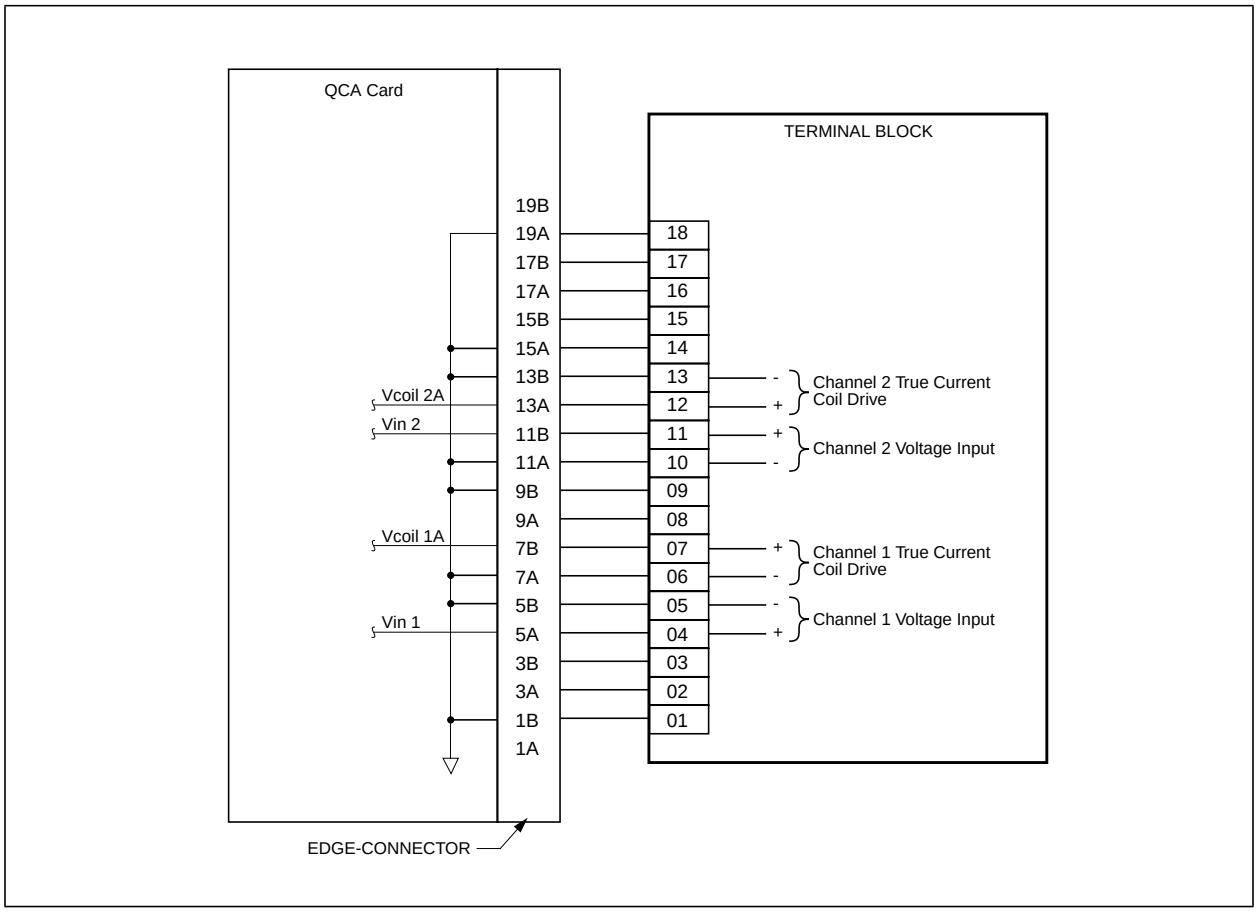
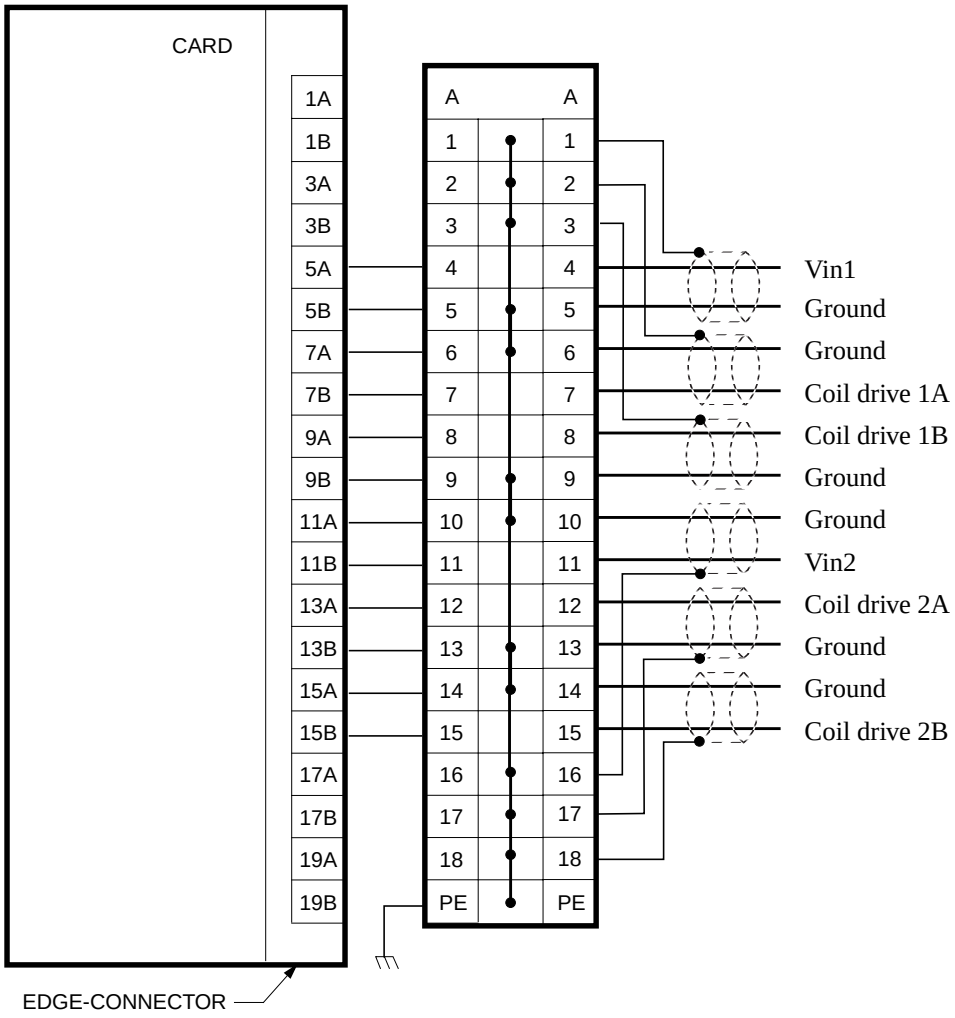


Figure 3-124. QCA Wiring Diagram (Group 2)
(Using AMP-18 conductor 18 AWG wiring) (3A99512)

For CE MARK Certified System

3 of 3



Notes

1. The A and B cabinets **MUST** be bolted together to use the QCA in CE Mark Certified Systems.

2. As shown, the shields and grounds must be connected together and to earth ground at the B cabinet.

Figure 3-125. QCA CE MARK Wiring Diagram

3-17. QCI

Contact Input
(Style 7379A06G02)

3-17.1. Description

Group 02 is applicable for use in the CE MARK Certified System

The QCI provides 16 digital contact inputs and a +48 V contact-wetting supply voltage (see Figure 3-126). This contact-wetting voltage provides supply isolation and reduced current power consumption due to the current limiting capability of the supply. The QCI digitally filters the contact-input signals and provides the option of inverting the polarity of any data bit.

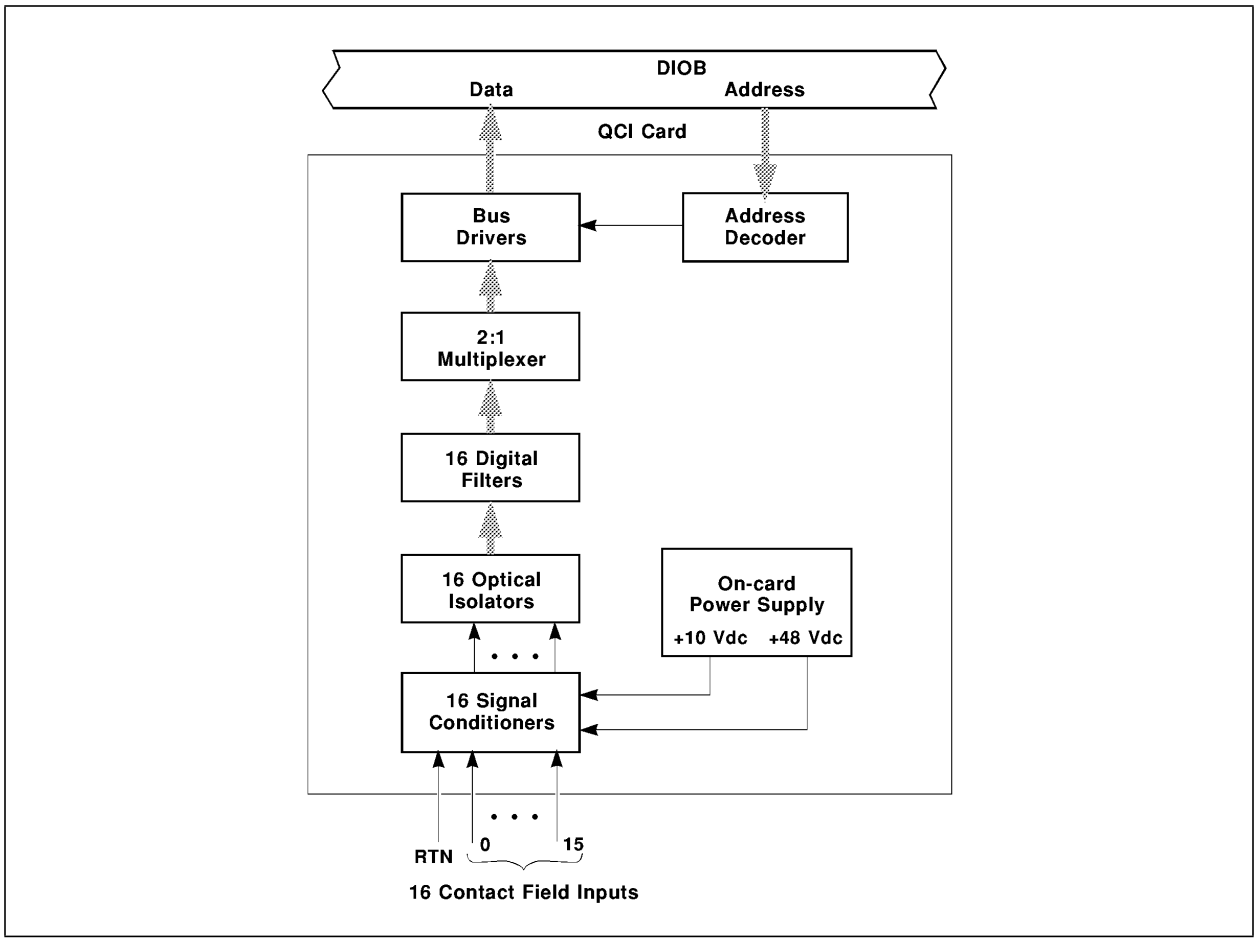


Figure 3-126. QCI Block Diagram

3-17.2. Features

The QCI card is available in two groups and provides the following features:

- Dual on-card contact-wetting power supply for low power consumption
- Separate status-indicating LEDs for each input
- Compatible with any DIOB controller
- IEEE surge-withstand protection
- Optical isolation for each input
- Optional digital switch selectable polarity of each bit

The Group 2 QCI provides 16 digitally-filtered contact inputs sharing a common return line with the ability to invert data-bit polarity (G01 does not have this option and is no longer manufactured).

3-17.3. Specifications

A functional block diagram of the QCI is shown in Figure 3-127.

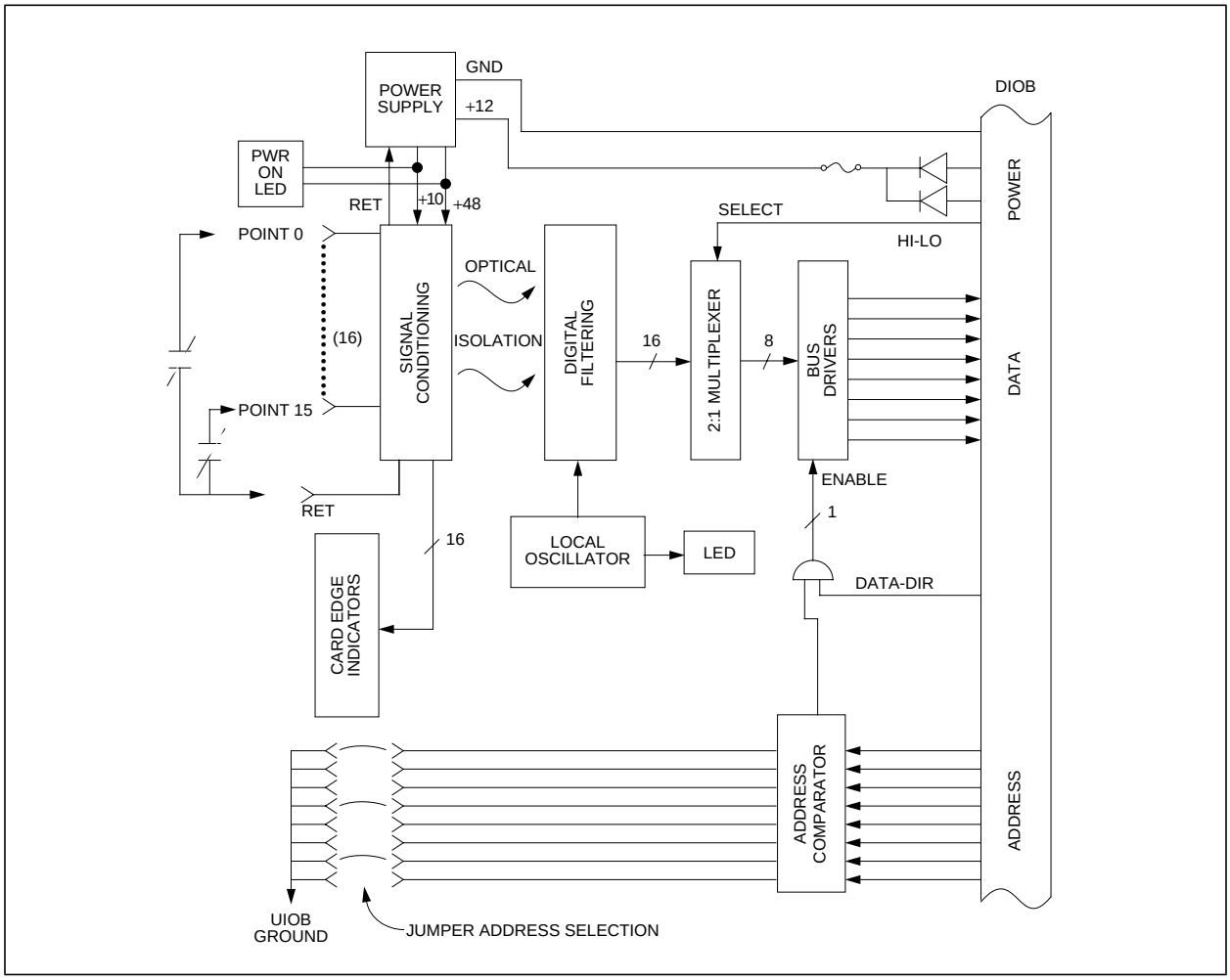


Figure 3-127. QCI Card Block Diagram

Input Requirements

Digital Filter Delay:2.6 msec to 6.0 msec

Input Signal Rejection

Input signal duration <2.6 msec is always rejected.
Input signal duration >6.0 msec is always passed.

Note

The elapsed time between the contact's opening and its subsequent closure must be >15 msec.

Contact leakage resistance:50 KΩ minimum.

Table 3-83. QCI Contact Wetting Voltage

Parameter	Minimum	Nominal	Maximum
Open Circuit Voltage	42V	48V	56V
Closed Contact Current	6mA	14mA	22mA

Input Capabilities

The signal lines at the DIOB interface are specified by the DIOB specifications description.

Power Supply

Primary: +13 V ±0.1 Vdc

Backup: +12.6 V ± 0.2 Vdc

Current: 500 mA (maximum) supplied by DIOB

Power Consumption: 6.3 W (maximum)

Electrical Environment

IEEE Surge withstand capability

Common Mode Voltage: 500 Vdc or peak ac (line frequency)

Card Addressing and Data Output

The QCI card address is established by eight jumpers on the front card-edge connector as shown in Figure 3-128. The insertion of a jumper encodes a "1" on the address line.

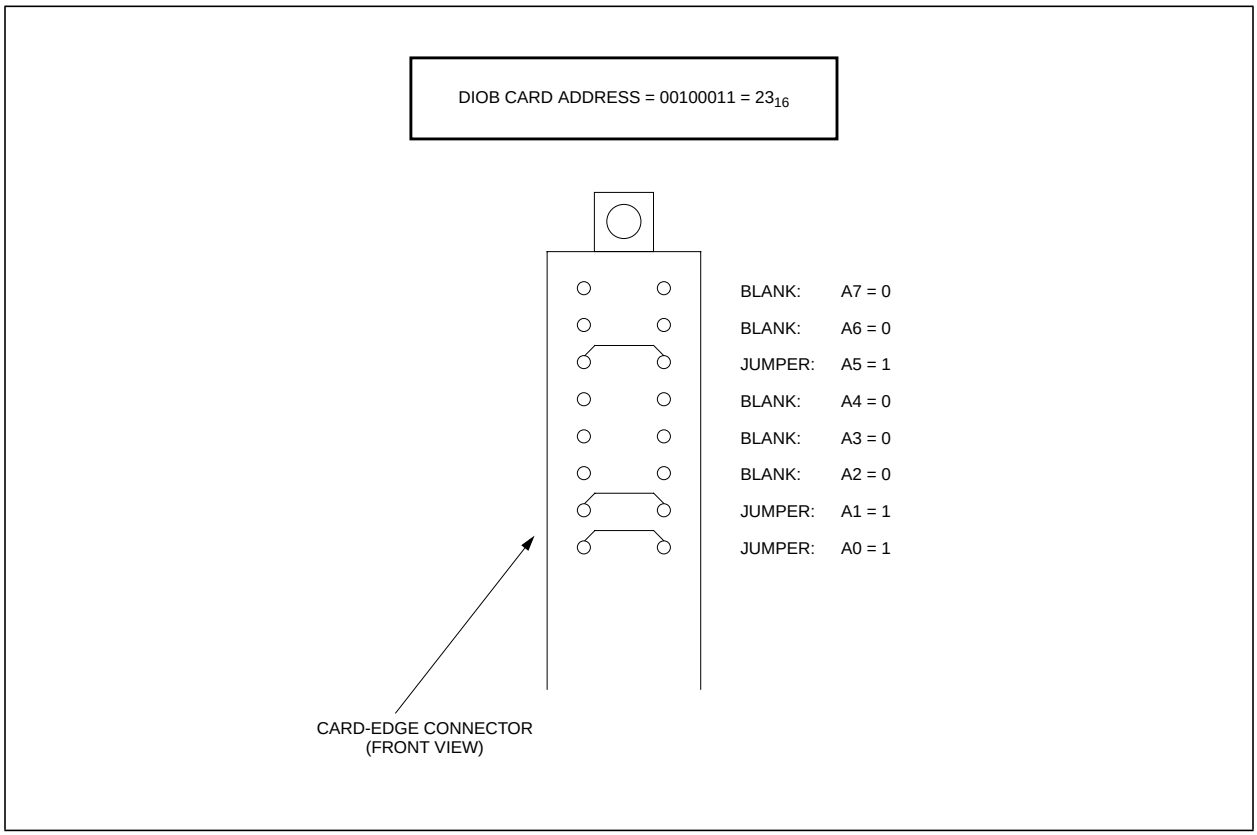


Figure 3-128. QCI Card Address Jumper Assembly

The binary data that is sent to the system controller over the DIOB are the 16 data bits from the 16 contact inputs divided into two eight-bit bytes.

Connections and Field Cabling

Refer to Figure 3-129 for details regarding the following discussion.

Up to 1.2 mA may flow through any contact shunt resistance from the +48V supply (with open contacts, no current can flow from the +10V supply due to reverse-biased diodes). A resistance of 50 KΩ (minimum) is required to maintain the high-level contact-wetting voltage. However, the contacts are recognized as open with a shunt resistance of 10 KΩ (minimum). To ensure that closed contacts are always recognized as closed, the following equation must be applied:

$R_C + R_{LINE} + 16R_R \leq 60\ \Omega$

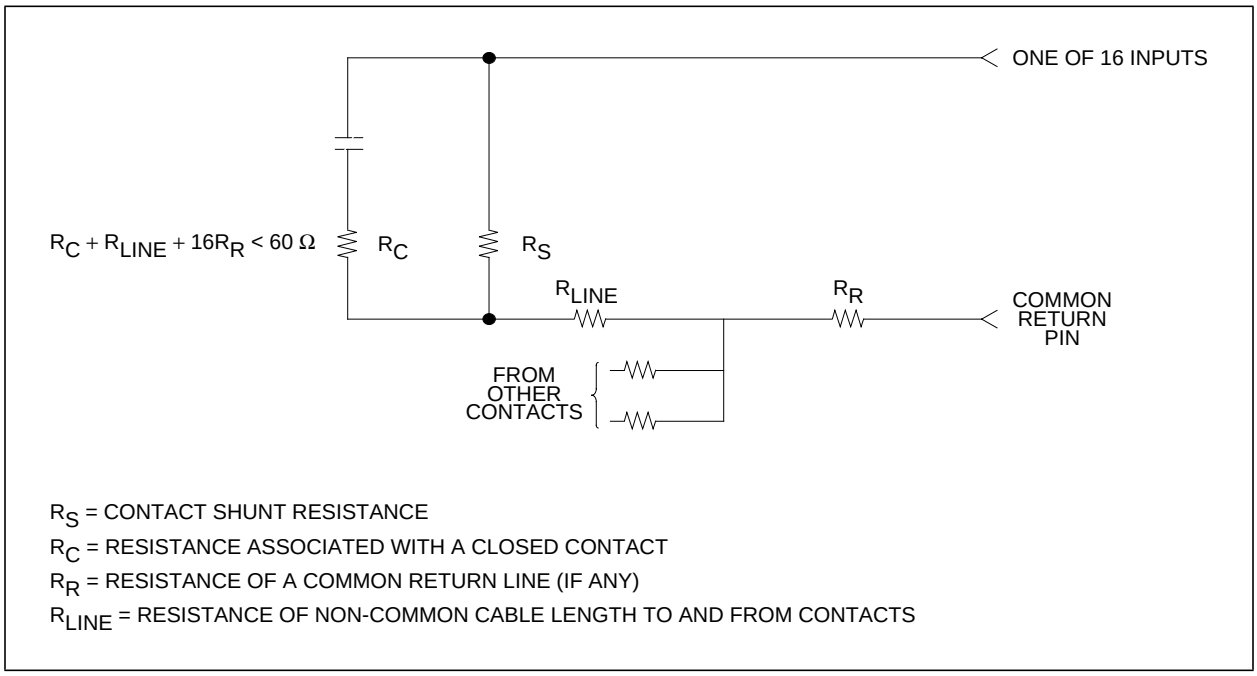


Figure 3-129. Cable Length Limitations for QCI Card

Contact Cycle Time

If the maximum QCI on card generated voltage is to be applied to plant contacts that interface to the QCI card, the elapsed time between a contact opening and its subsequent closure must be greater than 15 msec.

Table 3-84 gives the cable length limits for various gauges of wire.

Table 3-84. Cable Length Limits for QCI Card

Gauge	Ohms/ thousand ft	16 Commons/Card (thousand ft) (maximum)[1]	1 Common/ Card (ft) (maximum)[2]
8	0.654	92	5,400
10	1.04	58	3,400
12	1.66	36	2,140
14	2.27	26	1,560
16	4.18	14	845
18	6.64	9.0	530
20	10.2	5.9	345
22	16.2	3.7	215

[1]The maximum cable length for a 16-common/card assumes that $R_R = 0$ and $R_C = 0$. The length given is the sum of the lengths to and from the contacts.

[2]The maximum cable length for a 1-common/card assumes that $R_C = 0$. The length of the return is equal to the length of the cable to the contact. The length given is the length to the contact only.

The QCI pin assignments are given in Table 3-85. These pins are located on the front-edge connector.

Table 3-85. QCI Pin Assignments

Connection Pins	B Side (Component Side)	A Side (Solder Side)
28	$\overline{A7}$	GND
27	$\overline{A6}$	GND
26	$\overline{A5}$	GND
25	$\overline{A4}$	GND
24	$\overline{A3}$	GND
23	$\overline{A2}$	GND
22	$\overline{A1}$	GND
21	$\overline{A0}$	GND
20		
19		
18		
17	B15	B14
16		
15	B13	B12
14		
13	B11	B10
12		
11	B9	B8
10		
9	B7	B6
8		
7	B5	B4
6		
5	B3	B2
4		
3	B1	B0
2		
1	RET	RET

Controls and Indicators

QCI Group 2 (G02) provides the ability to reverse the polarity of the data bits depending on switch setting. Table 3-86 gives the data bit values for switch positions.

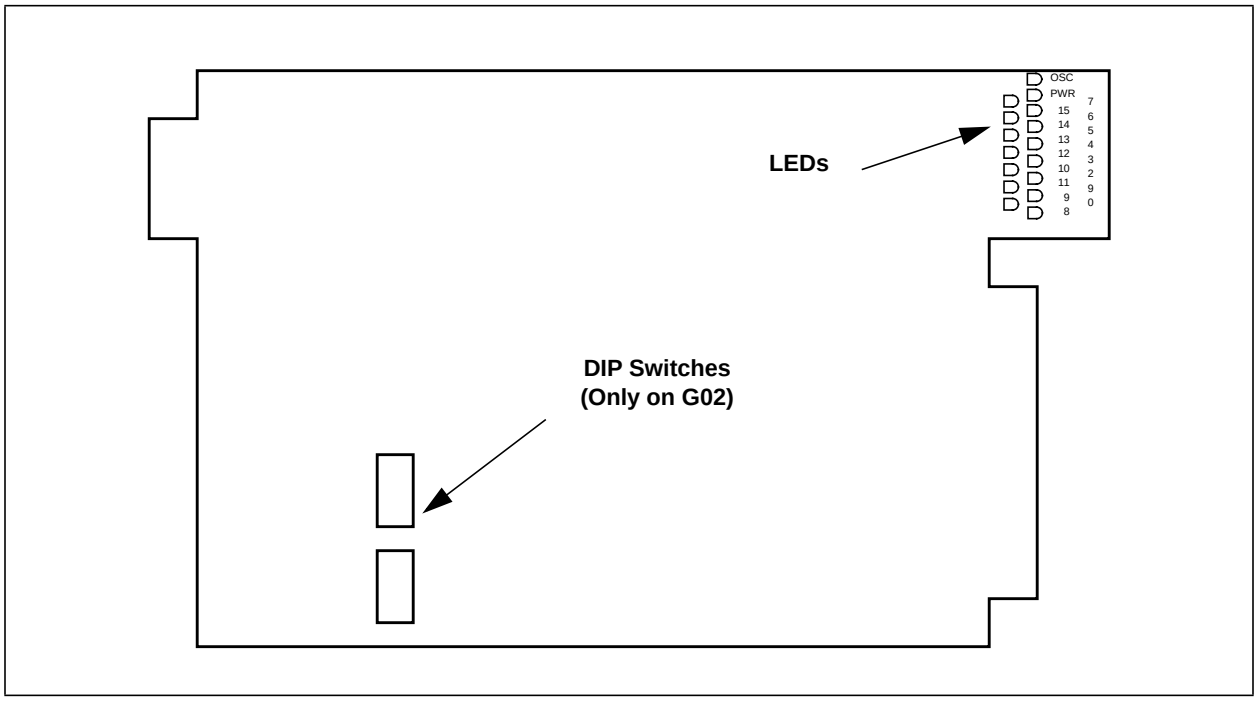


Figure 3-130. QCI Card Components

Separate status-indicating LEDs for each contact input are located at the front of the card (see Figure 3-130).

Table 3-86. QCI G02 DIP Switch Positions

Switch Position	Contact State	Digital Value
OPEN	Open Closed	0 1
CLOSED	Open Closed	1 0

3-17.4. Installation Data Sheet

1 of 2

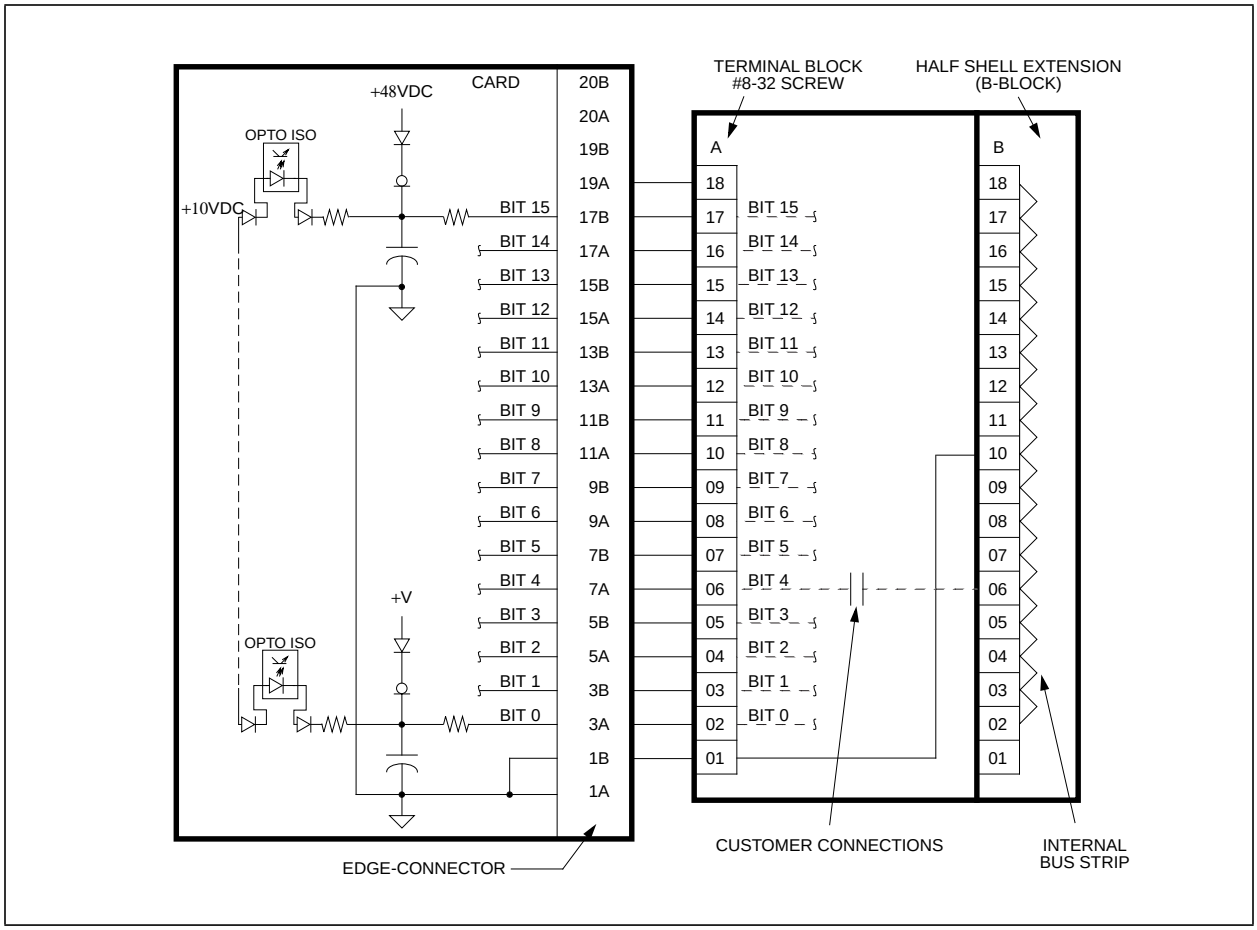


Figure 3-131. QCI Wiring Diagram

For CE MARK Certified System

2 of 2

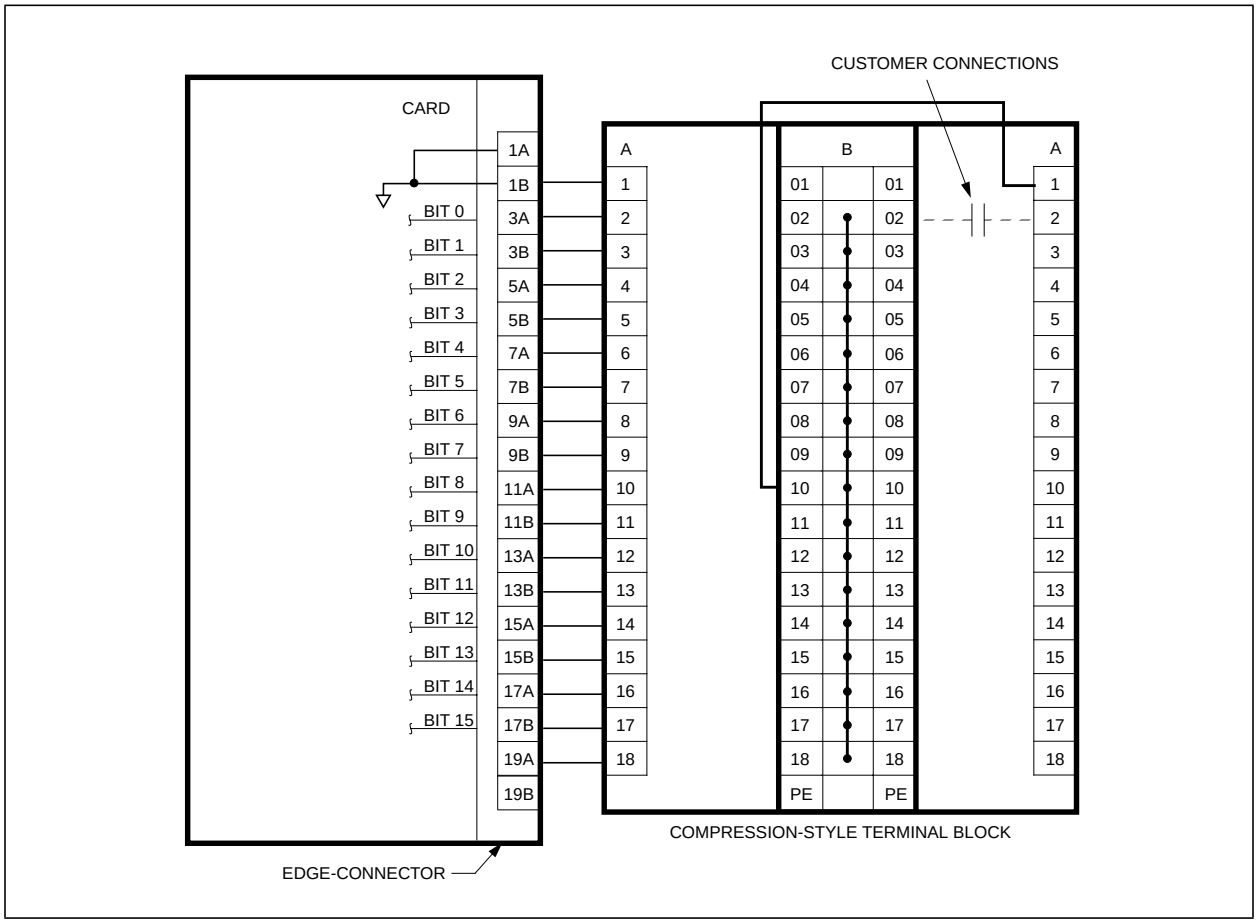


Figure 3-132. QCI CE MARK Wiring Diagram

3-18. QDC

Q-Line Digital Controller
(Style 4256A15G01 through G11)

3-18.1. Description

G01 and G02 are applicable for use in the CE MARK Certified System

The Q-Line Digital Controller (QDC) printed circuit board provides an additional level of control capability, supplementing DPUs. The QDC has an on-board processor which controls outputs based on user-defined algorithms. Full details on the configuration and use of the QDC are contained in the "QDC User's Guide" (U0-1105).

3-19. QDI

Digital Input
(Style 2840A13G01 through G11)

3-19.1. Description

The QDI card had been superseded by the QID card. For new applications, refer to the following table to determine the equivalence between QID and QDI cards:

Table 3-87. QDI-QID Card Equivalents

QDI Group	Equivalent QID Group	Input Level	Inputs*
G02	G02	24 VAC/DC	8
G04	G04	48 VAC/DC	8
G06	G06	120 VAC/DC	8
G10	G10	48 VDC	16
G11	G11	120 VAC	8
* 16 means single-ended inputs, 8 means differential inputs.			

The QDI card provides signal conditioning for 16 digital voltage process inputs, and it interfaces these signals to the DIOB (see Figure 3-133). The QDI has two different kinds of voltage-sensing input circuits available. Cards can have eight two-wire (differential) inputs without electrical connections to other points, or sixteen single-ended inputs which share a common return line.

Block Diagram

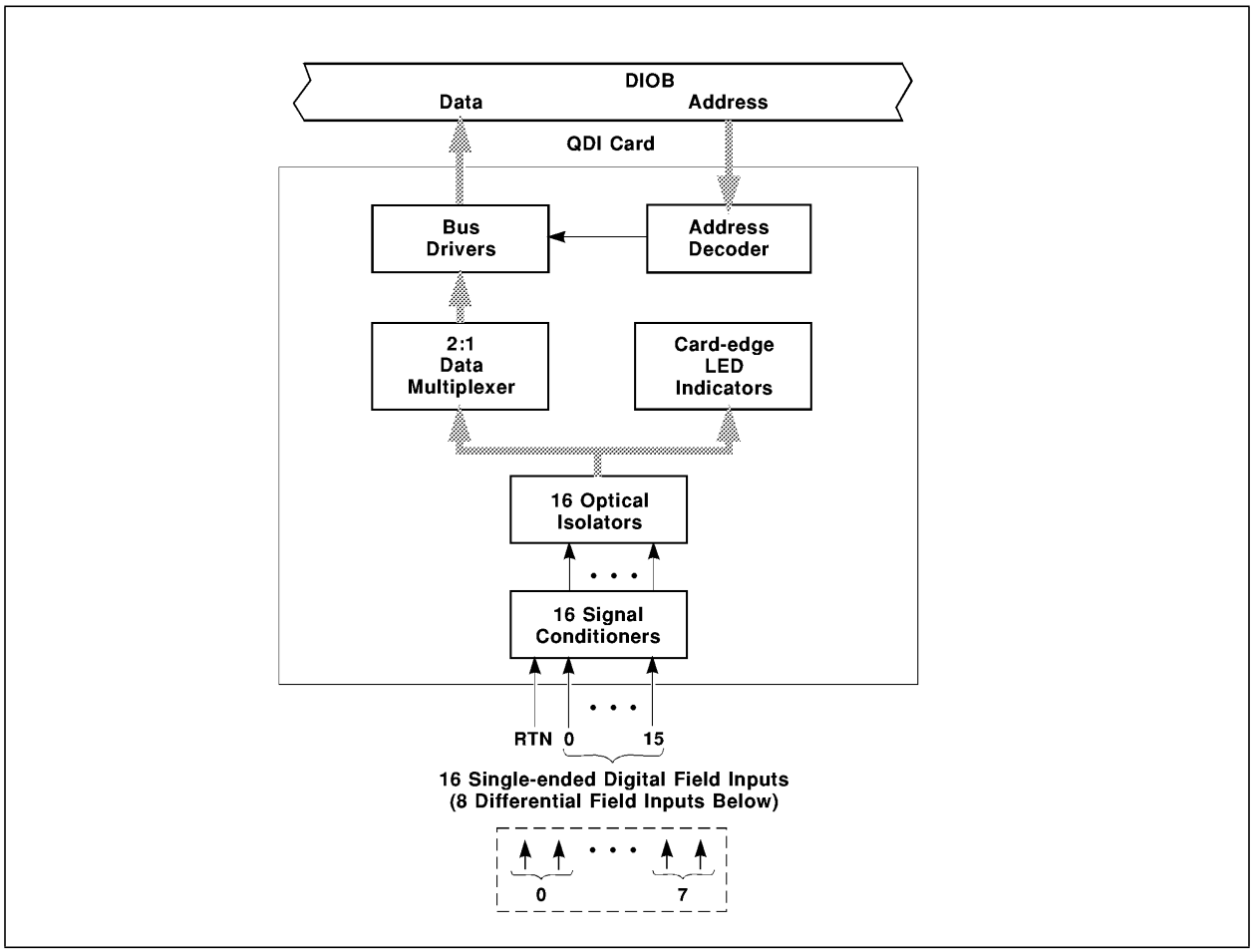


Figure 3-133. QDI Block Diagram

3-19.2. Features

The QDI card is available in 11 groups and provides the following features:

- G01 provides 16 single-ended 5 VDC inputs
- G02 provides eight 24 VAC/VDC differential inputs
- G03 provides 16 single-ended 24 VAC/VDC inputs
- G04 provides eight 48 VAC/VDC differential inputs
- G05 provides 16 single-ended 48 VAC/VDC inputs
- G06 provides eight 120 VAC/VDC differential inputs
- G07 provides 16 single-ended 120 VAC/VDC inputs

- G08 provides 16 single-ended logic-oriented, +12 VDC inputs
- G09 provides 16 single-ended non-logic (filtered), 12 VDC inputs
- G10 provides 16 single-ended 48 VDC inputs with filter circuitry for pulse input applications
- G11 provides eight 120 VAC/VDC differential inputs (high threshold)

3-19.3. Specifications

Input Requirements

Table 3-88. QDI Input Requirements

Group	ON Input Voltage (VDC or VAC rms) Min/Max		OFF Input Voltage (VDC or VAC rms) (max)	ON Input Current (mA) Min/Max		Propagation Time (msec) Min/Max		Power In Front End with All Units On, (Nominal Voltage) (Watts)
G01	4	6	0.9	10	15	–	0.2	1.0
G02	20	30	3	10	15	5	21	2.3
G03	20	30	3	10	15	5	21	4.6
G04	40	60	4	10	15	5	21	4.6
G05	40	60	4	10	15	5	21	9.2
G06	100	150	6	10	15	5	21	11.5
G07	100	150	6	10	15	5	21	23.0
G08	10	15	2	10	15	–	0.2	2.3
G09	10	15	2	10	15	5	21	2.3
G10	40	60	4	10	15	5	2.1	9.2
G11	100	150 VDC 145 VAC (rms)	31 VDC 25 VAC (rms)	10	15	5	43	10.1

Power Supply

Primary: +13.0 V $\pm$0.1 VDC/– 0.6 VDC

Backup: +13.0 V $\pm$ 0.1 VDC/– 0.6 VDC

Current: 200 mA (maximum for single-ended cards)
100 mA (maximum for differential cards)

Electrical Environment

IEEE Surge withstand capability

Common Mode Voltage: 500 VDC or peak AC (line frequency)

3-19.4. Card Addressing and Data Output

The QDI card address is established by eight jumpers on the front card-edge connector as shown in Figure 3-134 and Figure 3-135. The insertion of a jumper encodes a “1” on the address line.

The binary data that is sent to the system controller over the DIOB are the 8 or 16 data bits from the field inputs. For differential inputs, one byte of data is sent over the DIOB (Figure 3-134). For single-ended inputs, two bytes of data are sent over the DIOB (Figure 3-135).

This parameter defines the color for the value when the point is in alarm.

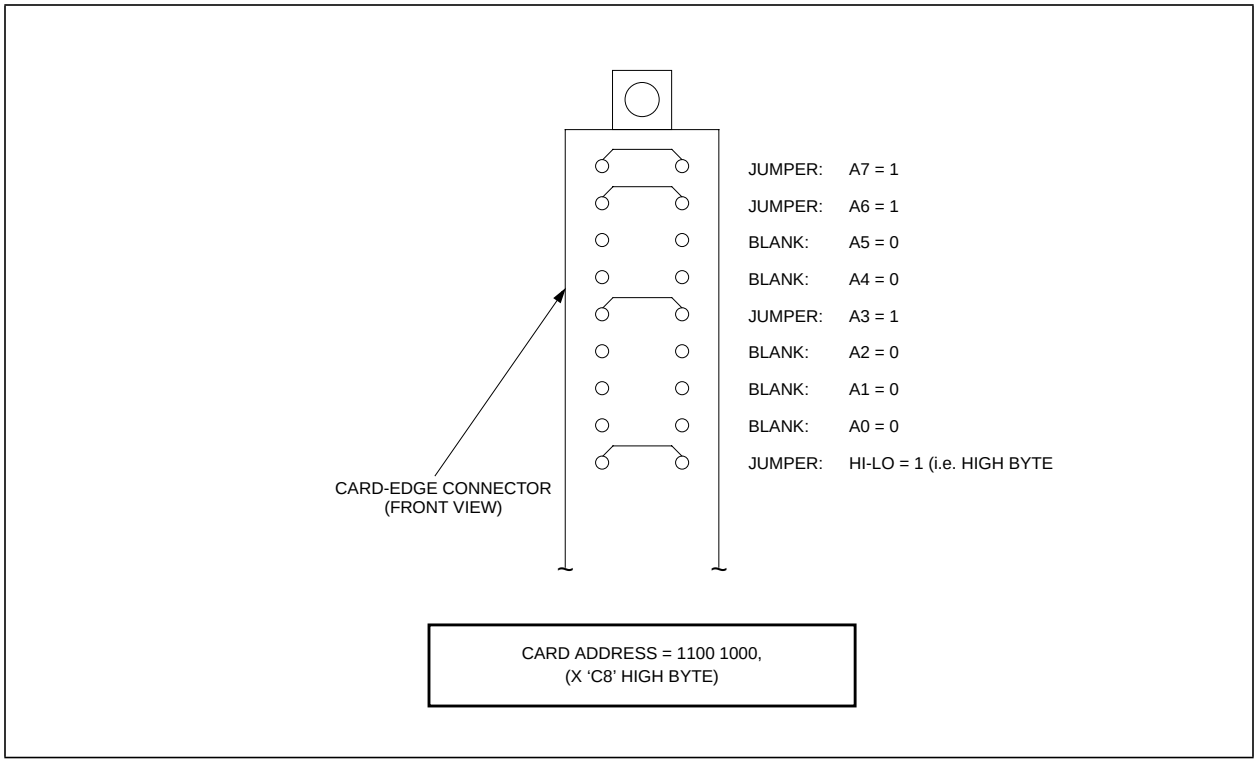


Figure 3-134. QDI Card Address Jumper Assembly (Differential Input)

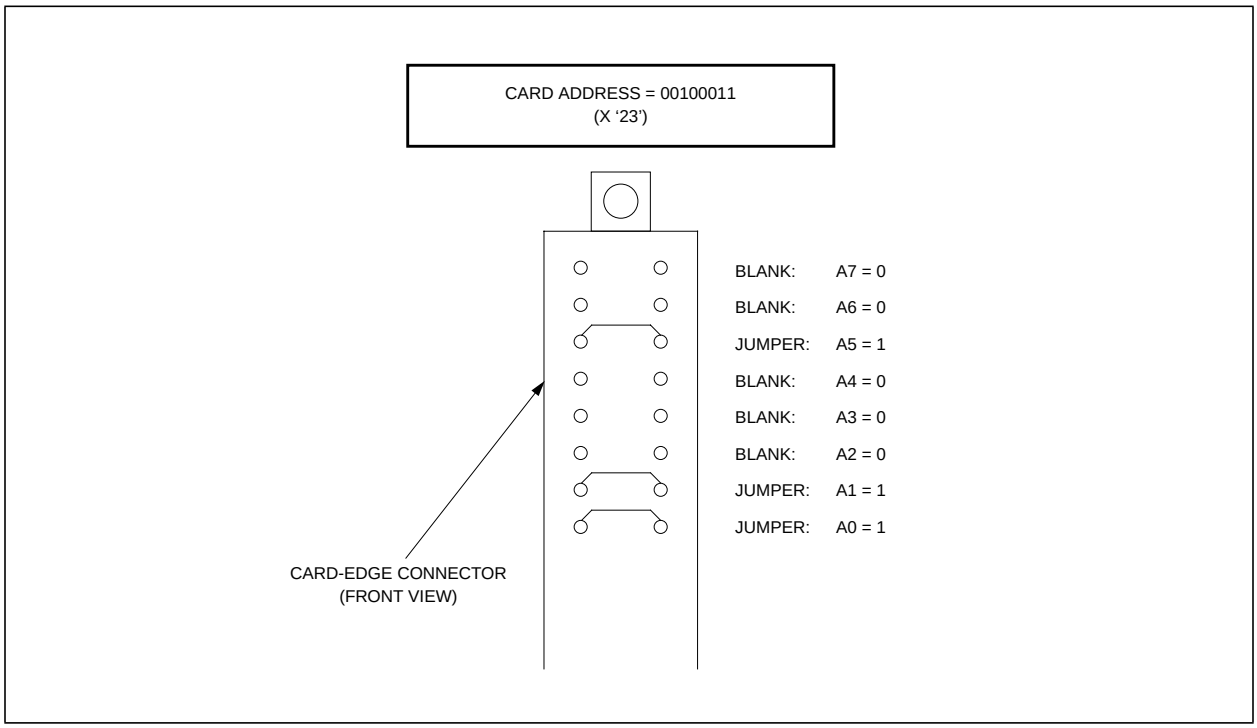


Figure 3-135. QDI Card Address Jumper Assembly, Single Ended Input

Connections and Field Cabling

The digital inputs enter to the QDI Card on the front-edge connector. The pin assignments for this connector are listed in Table 3-89.

Figure 3-136 shows the wiring for point inputs to a G01. Figure 3-137 shows the typical wiring for the single-ended input groups.

The cable length to field contacts is limited by cable capacitance when AC is used to wet contacts. See Table 3-90.

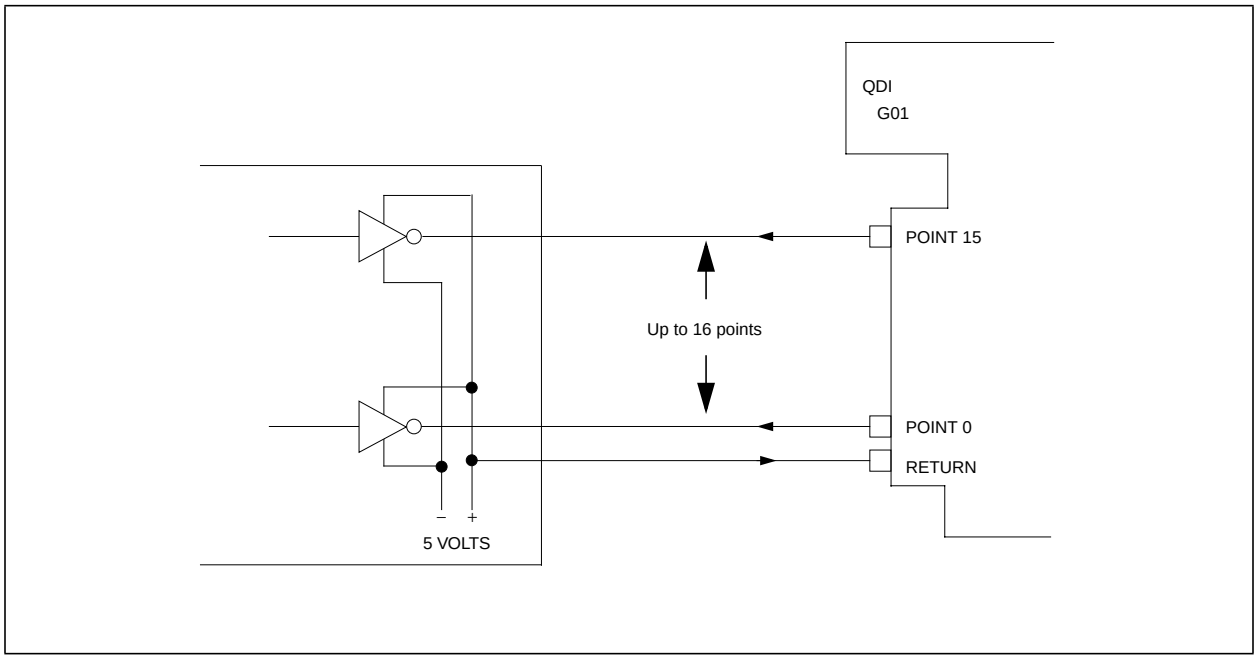


Figure 3-136. QDI G01 Point Wiring

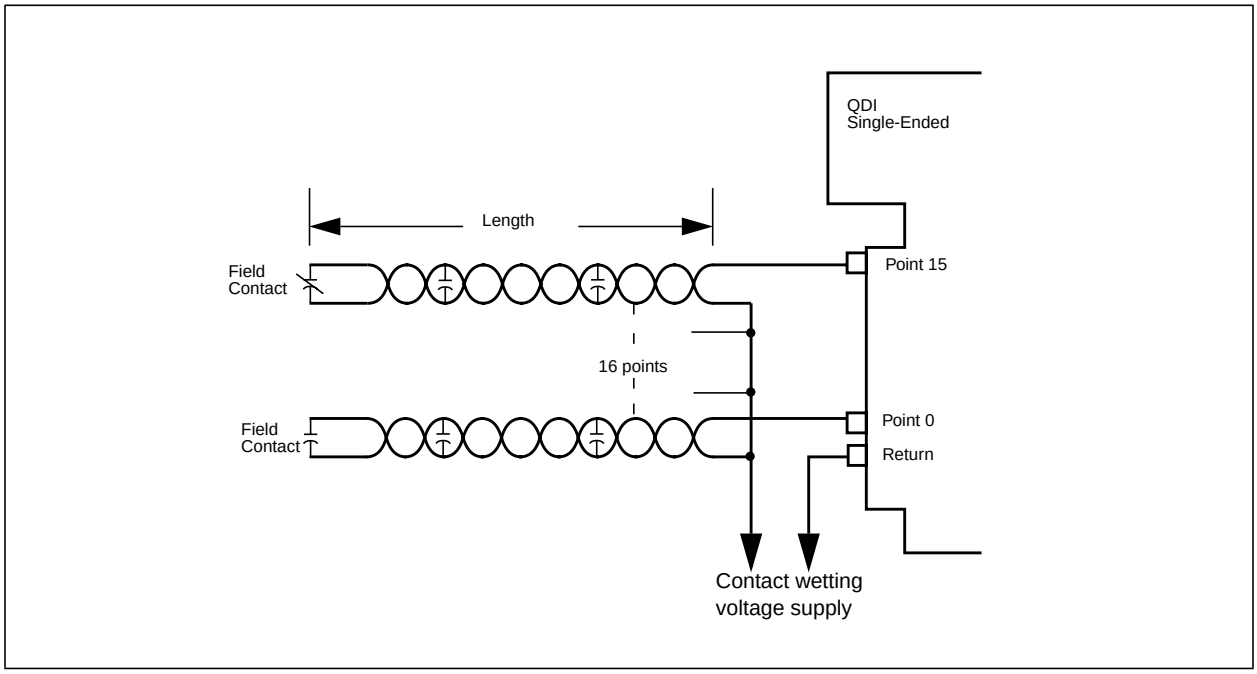


Figure 3-137. QDI Typical Contact Input Point Wiring (G03, 05, 07, 08, 09, 10)

Table 3-89. QDI Pin Allocations

(G01, G03, G05, G07, G08, G09, G10)		
Input Digital Bit	**PC Card Edge Pin**	**Field Terminal Block Terminal Number**
Return	1A and 1B	1
Bit 15	17B	17
14	15A	14
13	13B	13
12	11A	10
11	9B	9
10	7A	6
9	5B	5
8	3A	2
7	17A	16
6	15B	15
5	13A	12
4	11B	11
3	9A	8
2	7B	7
1	5A	4
0	3B	3

Table 3-89. QDI Pin Allocations (Cont'd)

(G02, G04, G06, G11)		
Input Digital Bit	**PC Card Edge Pin**	**Field Terminal Block Terminal Number**
Return	1A and 1B	1
Bit 0	3A	2
	3B	3
1	5A	4
	5B	5
2	7A	6
	7B	7
3	9A	8
	9B	9
4	11A	10
	11B	11
5	13A	12
	13B	13
6	15A	14
	15B	15
7	17A	16
	17B	17

Table 3-90. Cable Length for QDI

Group	Maximum Capacitance	At 50 pF/Ft typical capacitance Maximum Cable Length
G02 (24 VAC)	60,000 pF	1000 ft.
G04 (48 VAC)	30,000 pF	500 ft.
G06 (120 VAC)	15,000 pF	250 ft.
G11 (120 VAC)	15,000 pF	250 ft.

3-19.5. Controls and Indicators

Separate status-indicating LED’s for each input are located at the front of the card (see Figure 3-138).

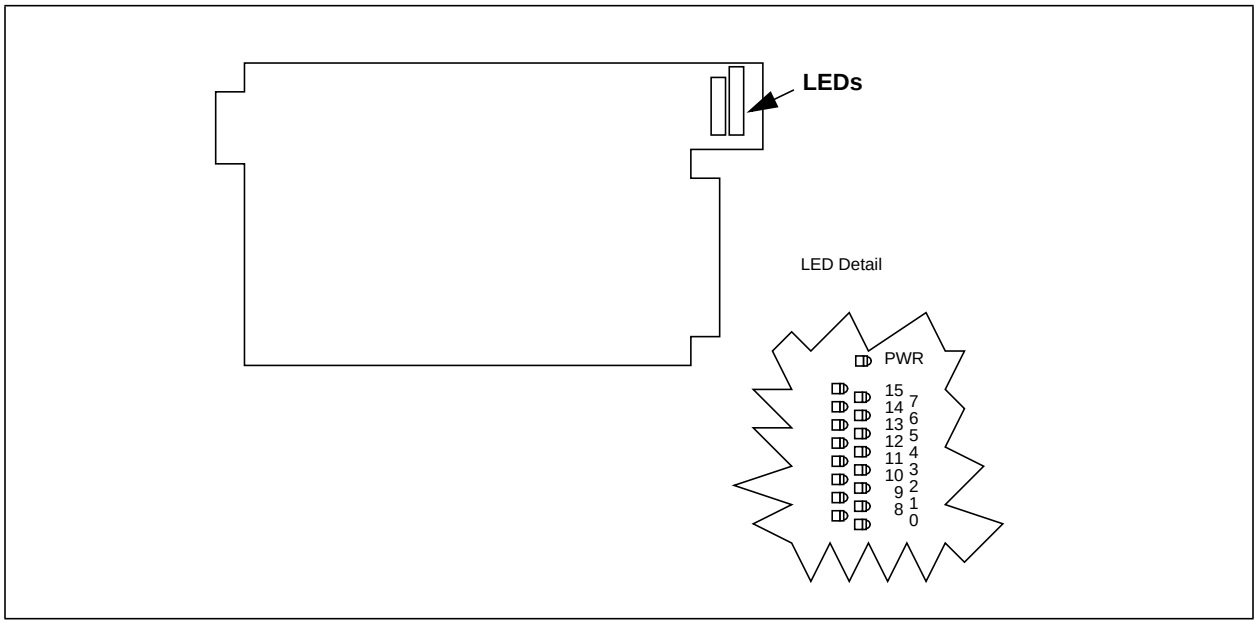


Figure 3-138. QDI Card Components

3-19.6. Installation Data Sheet

1 of 1

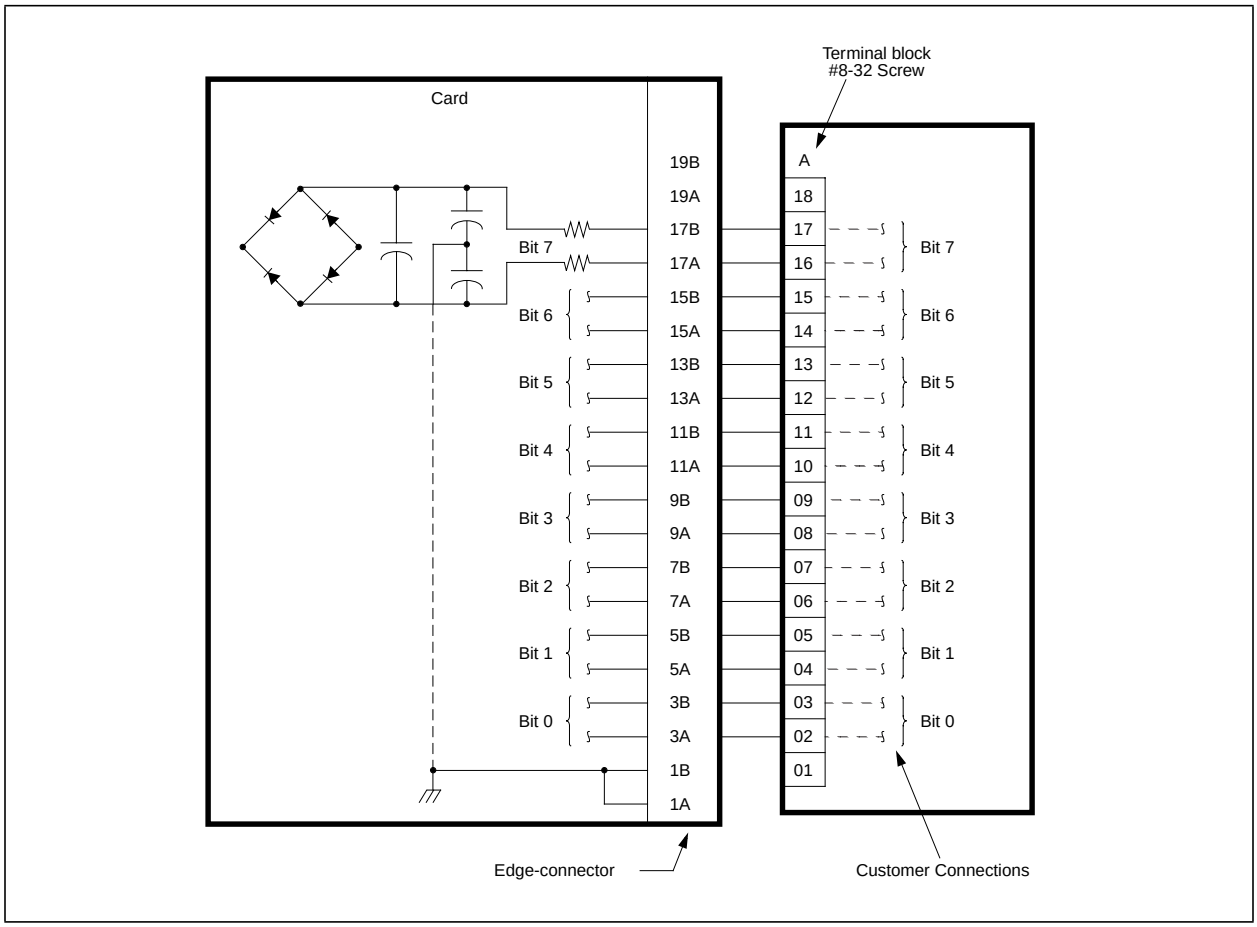


Figure 3-139. Wiring Diagram: QDI Groups 2, 4, 6, and 11

3-20. QDT

Diagnostic Test
(Style 7379A29G01)

3-20.1. Description

Applicable for use in the CE MARK Certified System

The Q-line Diagnostic Test (QDT) card is a DIOB testing device which verifies that a system's DIOB functions properly (see Figure 3-140). To do this, this card verifies the integrity of the DIOB data, address and control lines. Additionally, this card verifies that the DIOB controller can drive the DIOB and related point cards mounted on it. In a process control system, the Q-line point cards are used for signal conditioning.

These point cards convert analog or digital field signals from a process into equivalent digital signals that are compatible with the supervising controller. Q-line point cards interface to a controller via the DIOB, which provides a byte oriented digital exchange of process information. The QDT card provides for diagnostic testing of this interface.

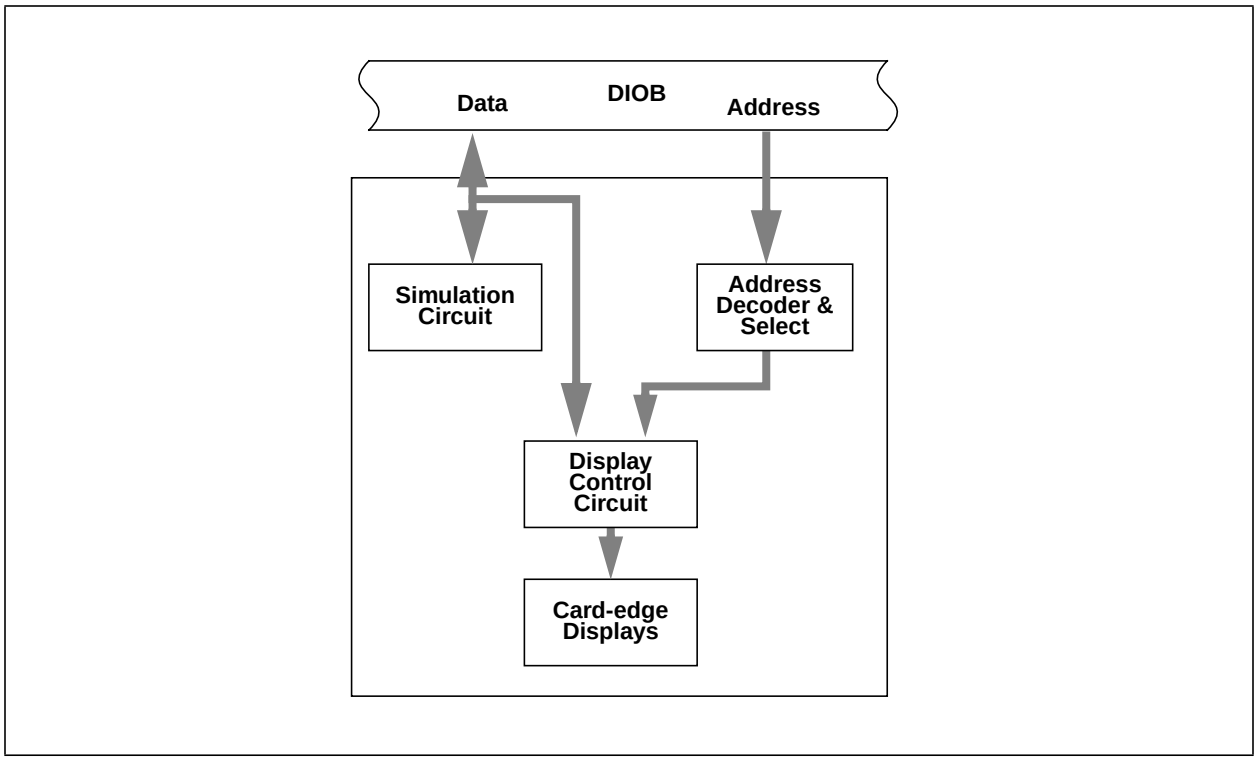


Figure 3-140. QDT Block Diagram

3-20.2. Features

The QDT card is available in one group and provides the following features:

- Card-edge switches for mode selection and diagnostic testing.
- Simulates DC loading for 48 point cards.
- On-card 512 byte RAM to test the DIOB controller's addressing and bus driving ability.
- Card-edge LED's for data display.
- Automatic Display mode selection on power-up to protect an active DIOB from overloading.

Electrical connection to the QDT card is made through a 34-pin DIOB backpanel connector.

The QDT card may be housed as follows:

- In the standard Q-line card crate
- Mounted to crate with a M4X6MM screw (not provided with QDT card)

Operation

The QDT card provides two modes of operation:

- Simulator Mode – used to test DIOB and controller

Note

All point cards must be removed from the DIOB prior to Simulator mode operation.

- Display Mode – used to monitor a user selected DIOB address, displaying any data written to or read from the selected address.

Note

In the display mode, the user selects whether output or input data is to be displayed, via the card edge Data Direction switch.

3-20.3. Specifications

Power Requirements

- Voltage from DIOB:

Primary: +12.4 VDC to +13.1 VDC

Secondary: +12.4 VDC to +13.1 VDC

- Current from DIOB:

  750 mA maximum

- 5 VDC Power Supply:

  Derived internally on QDT card from 12 VDC supplied from DIOB

  Voltage: 4.8 VDC to 5.2 VDC

  Current: 400 mA maximum

Simulator Mode

In the Simulator mode, the QDT card tests that the DIOB controller is able to drive a DIOB of maximum length and with the maximum number of point cards plugged in. Additionally, the QDT card checks that the controller is able to address all possible DIOB locations and can generate the basic DIOB control signals.

The loading circuits, at the QDT card's DIOB signal inputs, simulate the DC loading of the point cards and the capacitance of the longest permissible DIOB (50 feet). DIOB signals must drop below 3 VDC to be recognized as a logic 0 or rise above 9 VDC to be recognized as a logic 1. These QDT input circuits contain voltage comparators with hysteresis to reject input DIOB signals with voltage levels between 3 and a 9 VDC.

In this mode, the QDT card (via the 512-bytes of RAM) tests the DIOB controller's DIOB addressing capability and the controller's ability to drive the DIOB. The QDT card's 512-byte RAM simulates the entire DIOB address space. Due to the fact that the QDT card simulates every DIOB point card address and the loading of a DIOB full of point cards, no other point card should be present on the DIOB/ controller combination being tested.

Therefore, to prevent any mishaps, when a QDT card is powered up or inserted into an active DIOB, it automatically powers up in the Display mode. The user then removes all other point cards from the DIOB before switching the QDT card into its Simulator mode. Two edge mounted LED's are provided to inform the user as to which mode the QDT card is in.

Caution

Failure to remove all point cards from the DIOB, prior to switching to the Simulator mode, can cause DIOB loading, generating a failed condition.

Also, in this mode, the QDT card generates a DEVICE BUSY pulse during every DIOB cycle. This DEVICE BUSY pulses generation may be disabled by the user via the card edge Device Busy enable switch. The DEVICE BUSY pulse is automatically disabled and not generated in the Display mode.

Display Mode

In the Display mode, the QDT card simply monitors the DIOB lines and displays data on sixteen card edge LED's. In this mode, the QDT logic does not interact with the DIOB address, data or control signal transfers.

Note

The QDT card displays DIOB data, while in the Simulator mode. However, no other point cards are permitted on the DIOB.

When the QDT card operates in the Display mode, it does not occupy any DIOB addresses and it appears to be transparent to the DIOB controller. All of the QDT logic, utilized for the Simulator mode, is isolated from the DIOB in the Display mode.

Sixteen of the QDT card's LED's are used to display the contents of a 16-bit DIOB data latch on the QDT card. This latch's contents are updated every time the selected DIOB address and direction of data (input or output) matches actual DIOB address and data direction. When this occurs, the appropriate LED's flash for approximately 0.1 seconds. In this way, the exchange of digital data between the Q-line point cards and the DIOB is monitored.

3-20.4. Controls and Indicators

The QDT card's controls and indicators are shown in Figure 3-141. Table 3-91 gives a description of these controls and indicators.

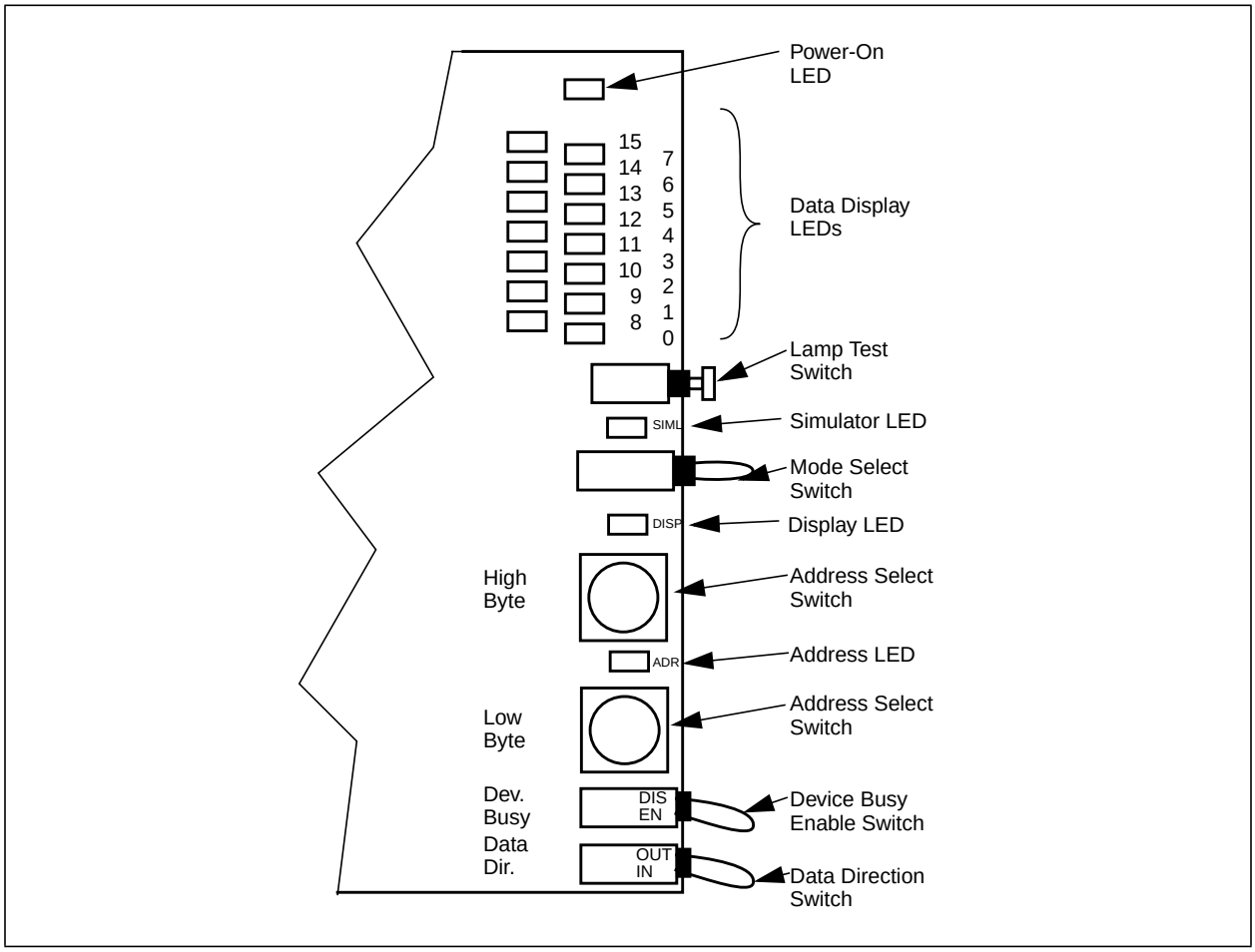


Figure 3-141. QDT Card Controls and Indicators

Table 3-91. QDT Card Controls and Indicators

Control/Indicator	Description
Power-on LED	Lights when QDT card is receiving power from DIOB.
Data Display LED's	These sixteen LED's are arranged in two rows of eight each. The row closest to the card edge displays the lower byte of DIOB data and the other row displays the higher byte of DIOB data.
Simulator LED	Lights when QDT card is operating in the Simulator mode.
Display LED	Lights when QDT card is operating in the Display mode.

Table 3-91. QDT Card Controls and Indicators (Cont'd)

Control/Indicator	Description
Address LED	Lights for approximately 0.1 seconds each time the DIOB address and data direction matches the address and data direction selected on the QDT card. **Note** When the addresses and data directions of the DIOB and QDT card repeatedly match, this LED appears to constantly light.
Lamp Test Pushbutton	Simultaneously tests all twenty QDT card LED's. When pressed, all LED's should light.
Mode Select Toggle Switch (momentary contact)	Selects the QDT card's operating mode. Pressing this switch toward DISP displaces the QDT card into the Display mode and lights the Display LED. Pressing this switch toward SIML places the QDT card into the Simulator mode and lights the Simulator LED. **Caution** The Simulator mode should not be selected unless **all** point cards are removed from the DIOB and the appropriate DIOB controller diagnostic programming exits. Failure to remove all point cards, prior to switching to the Simulator mode, can cause DIOB loading, generating a failed condition. Additionally, the QDT card's Simulator mode is of no use unless the necessary controller diagnostic programs are present.
Address Select Rotary Switches (hex)	Selects the upper and lower bytes of the DIOB address that is to be monitored by the QDT card's display logic.
Device Busy Toggle Switch	Enables or disables the generation of the DEVICE BUSY signal while the QDT card is operating in the Simulator mode.
Data Direction Toggle Switch	Selects the direction of DIOB data (input or output) that is to be displayed by the QDT card's Display LED's. Pressing this switch to IN, displays data that is input to the DIOB controller. Pressing this switch to OUT, displays data that is written to a point card.

3-21. QFR

Remote I/O Fiber-Optic Interface
(Style 4256A51G01)

3-21.1. Description

Applicable for use in the CE MARK Certified System

The QFR printed circuit board links master to remote nodes for long range communication (up to 5,280 feet or 1,609 meters). The card provides signal conversion from electrical to optical and optical to electrical (one unit sends and receives). Full details on the configuration and use of the QFR are contained in the "Remote Q-Line Installation Manual" (M0-0054).

3-22. QIC

Q-Line DIOB Monitor
(Style 4256A83G01)

3-22.1. Description

The Q-Line DIOB Monitor (QIC) card adds the capability to monitor DIOB operations. This function is often used in WDPF systems where DIOB operations driven by one DIOB controller must be monitored by a second computer, in addition to the normal DIOB controller. The second computer may be a WDPF DPU or a W2500 I/O subsystem. Monitoring is typically a requirement when upgrading from a W2500 system to a WDPF system.

The card stores data transferred during read or write operations on the control DIOB and allows this data to be read by the second, monitor, DIOB. The data transferred over the bus is stored in shared memory on the card. Logic on the QIC card prevents memory contention from occurring.

The QIC card contains a second (monitor) DIOB port which allows read-only operations of the shared memory. The monitor DIOB may originate from one of three connectors on the QIC. There are two types of connectors:

- One WDPF DPU connector.
- Two connectors for a W2500 I/O subsystem.

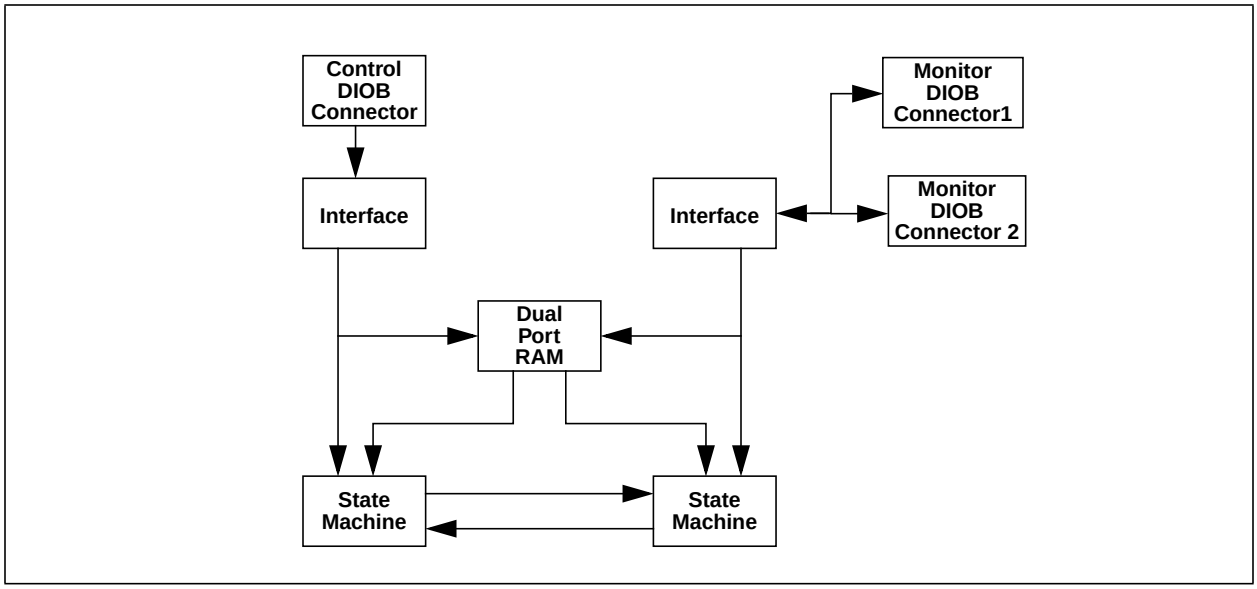


Figure 3-142. QIC Block Diagram

3-22.2. Features

DIOB 1 Operating Characteristics

- A DIOB 1 Read or Write operation to any location in the 512-byte DIOB address space causes the data present on the DIOB 1 data lines to be written into the Dual Port RAM at the address specified by the DIOB 1 address lines.
- The QIC will not drive the DIOB 1 data lines, regardless of whether a Read or Write operation is occurring.
- Device-Busy is checked on DIOB Read operation. If Device-Busy is not present at the proper time, no Data will be written into the shared RAM. On DIOB Write operation, Device-Busy is ignored. On Q-Line I/O cards which do not support Device-Busy, there is a jumper which to allow the Data be written to shared Ram on DIOB Read operation without valid Device-Busy. The jumper is shown in Figure 3-142.
- For double-byte (word) operations, the second (High) byte of data will be written to the RAM before the other (Read-only) port of the RAM may be accessed. This prevents data-tearing.
- DIOB specification, double-byte (word) operations must be accessed Low byte, then High byte, in order to prevent data-tearing.

DIOB 2 Operating Characteristics

- DIOB 2 Reads of any location in the 512-byte DIOB address space causes the data in the Dual Port RAM addressed by the DIOB 2 address lines to be driven onto the DIOB 2 data lines.
- DIOB 2 Writes are ignored.
- Device-Busy is supported by the QIC. DIOB 2 cycles are NOT extended.
- In compliance with the DIOB specification, double-byte (word) operations must be accessed Low byte, then High byte, in order to prevent the possibility of data-tearing.