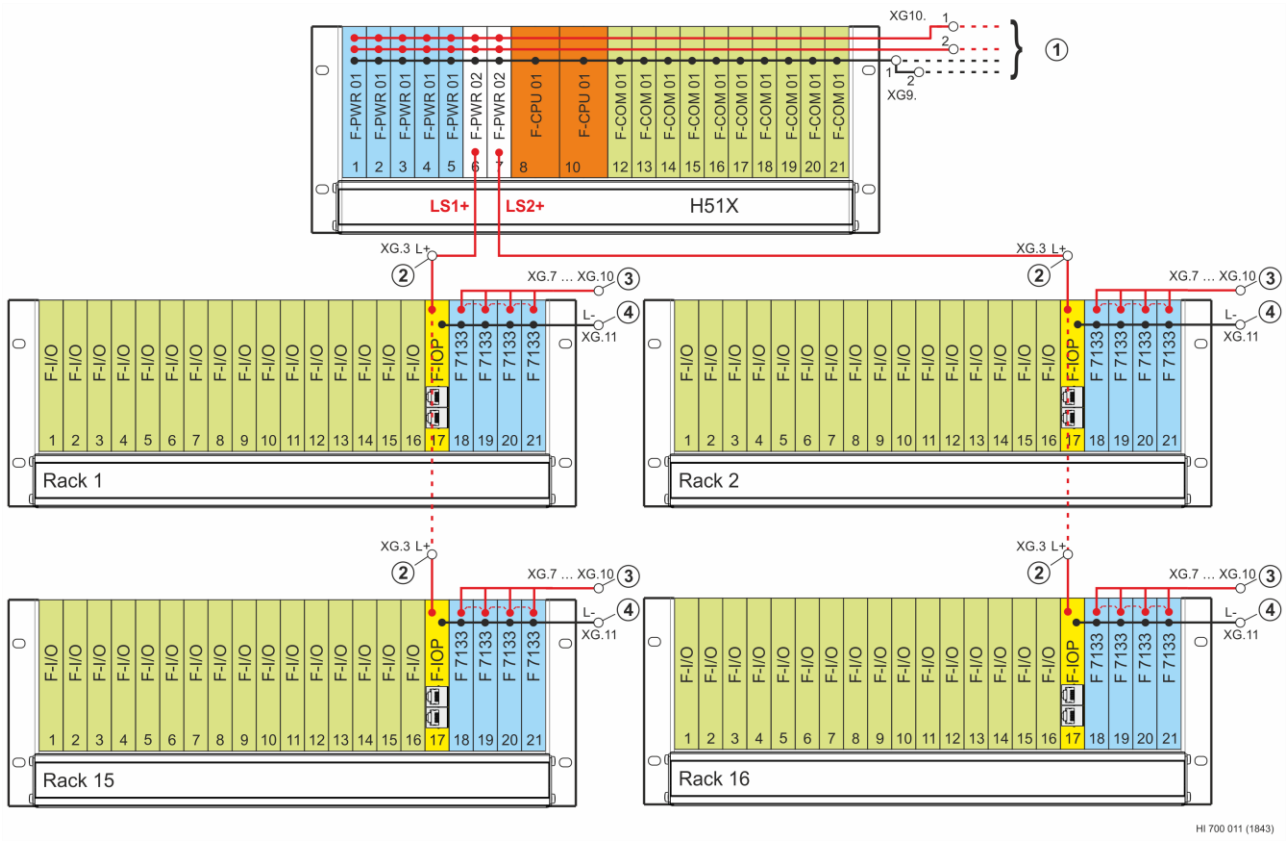
4.3.4 H51X Base Rack (24 VDC) I/O Level via F-PWR 02 Buffer Modules (Optional)

If the power supply units do not meet the requirements for protective separation and for compensating voltage failures of up to 20 ms such as specified in Chapter 4.3, or the requirements are > 20 ms, the buffer modules (F-PWR 02) can be used as an option to supply the I/O processing modules with 24 VDC.

In the following example, the buffer module in slot 6 compensates for voltage dropouts of I/O processing modules in the expansion racks with odd rack IDs. The buffer module in slot 7 compensates for voltage dropouts of the expansion racks with even rack IDs. In doing so, redundant I/O levels can be assembled based on the rack IDs. If one buffer module fails, operation of redundant racks is ensured via the remaining module. The failed buffer module must be replaced immediately to restore the original availability. This structure corresponds to that of the HIQuad HRS system.

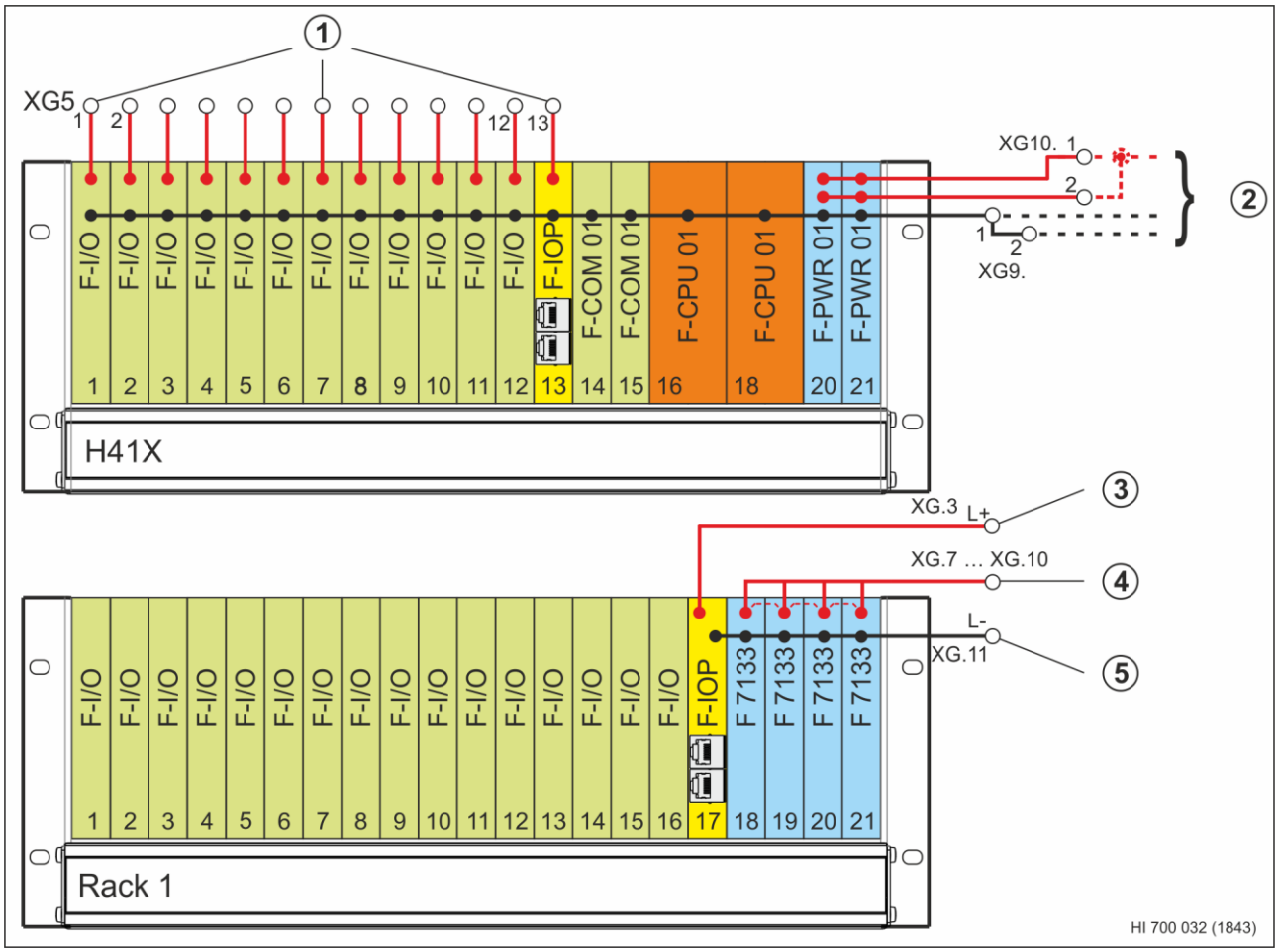


1. Connection to redundant power supply units, see Figure 20
2. Connection to the LS1+/LS2+ power supply of the F-PWR 02 buffer modules in accordance with the desired redundant structure of the I/O level
3. Redundant supply of the F 7133 power distribution modules, insert jumpers in accordance with the application
4. Reference potential L-

Figure 24: Mono Connection to H51X Base Rack (24 VDC)

4.3.5 Mono H41X Base Rack (24 VDC)

The 24 V mono power supply is performed for the H41X base rack and the I/O processing modules by connecting to one or redundant power supply units, see Figure 19.



1 Inline terminals XG5.1…XG5.13 to 24 V power supply, XG5.13 for connecting to the I/O processing modules.

2 Connection to one or redundant power supply units, see Figure 19

3 Connection to 24 VDC for the I/O processing module from the same source as the H41X base rack

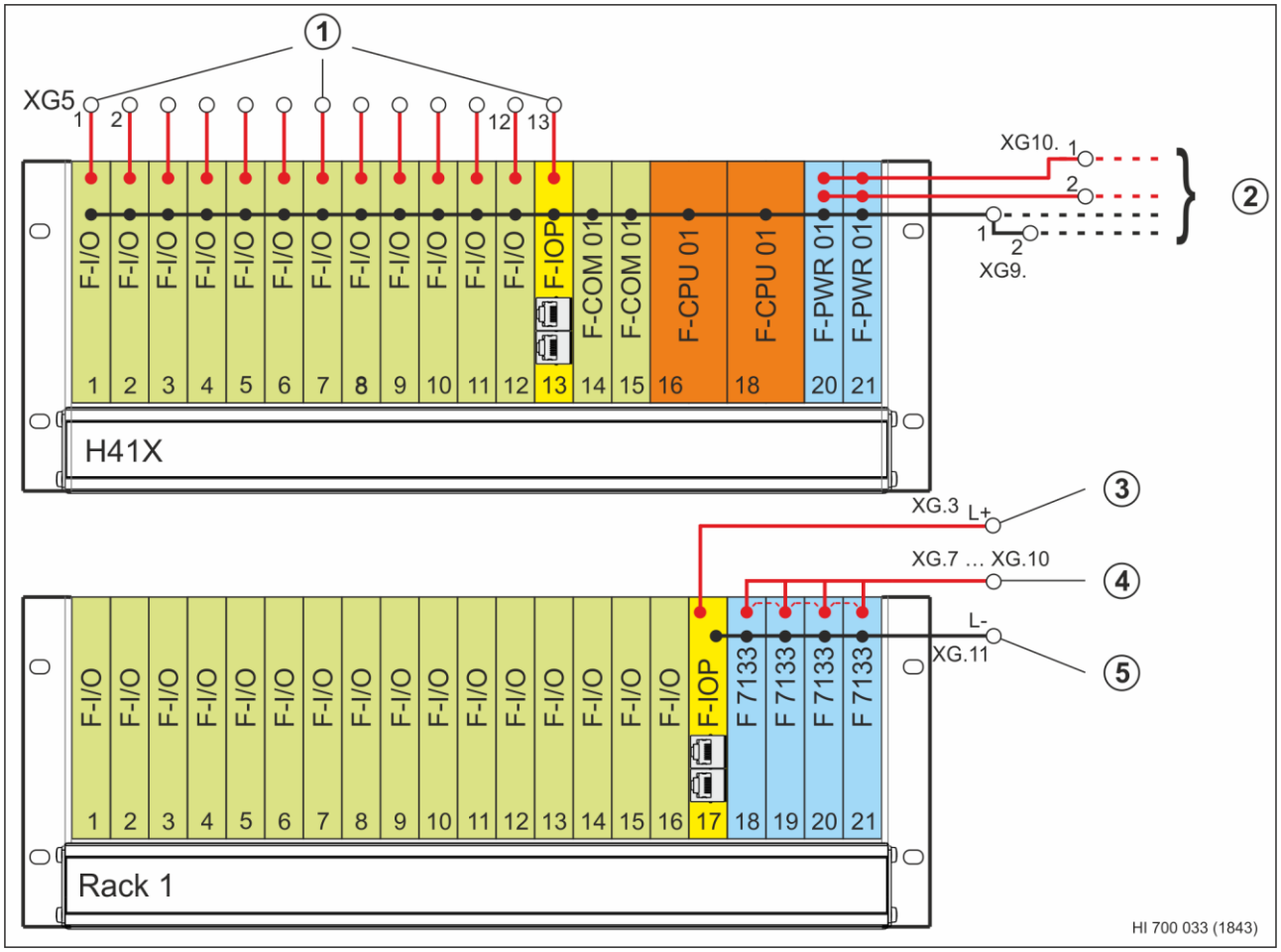
4 Redundant supply of the F 7133 power distribution modules, insert jumpers in accordance with the application

5 Reference potential L-

Figure 25: Mono Connection to H41X Base Rack

4.3.6 Redundant H41X Base Rack (24 VDC)

The I/O processing module in the H41X base rack and that in the extension rack must be powered from different power supply units to implement redundant I/O levels in the HIQuad H41X system. To this end, e.g., the I/O processing module in the H41X base rack can be connected to L1+ (terminal XG5.13) and the I/O processing module in the extension rack (terminals XG.3, L+), see Figure 20. The power supply units must be able to bridge voltage dropouts of up to 20 ms.



1. Inline terminals XG5.1…XG5.13 to 24 V power supply, XG5.13 for connecting to the I/O processing module in the H41X base rack
2. Connection to redundant power supply units, see Figure 20
3. Terminal XG.3 (L+) for connecting to 24 VDC for the I/O processing module in extension rack 1
4. Redundant power supply of the F 7133 power distribution modules, insert jumpers in accordance with the application
5. Reference potential L-

Figure 26: Redundant Connection to H41X Base Rack and Extension Rack 1

4.3.7 24 V Distribution for HIQuad X

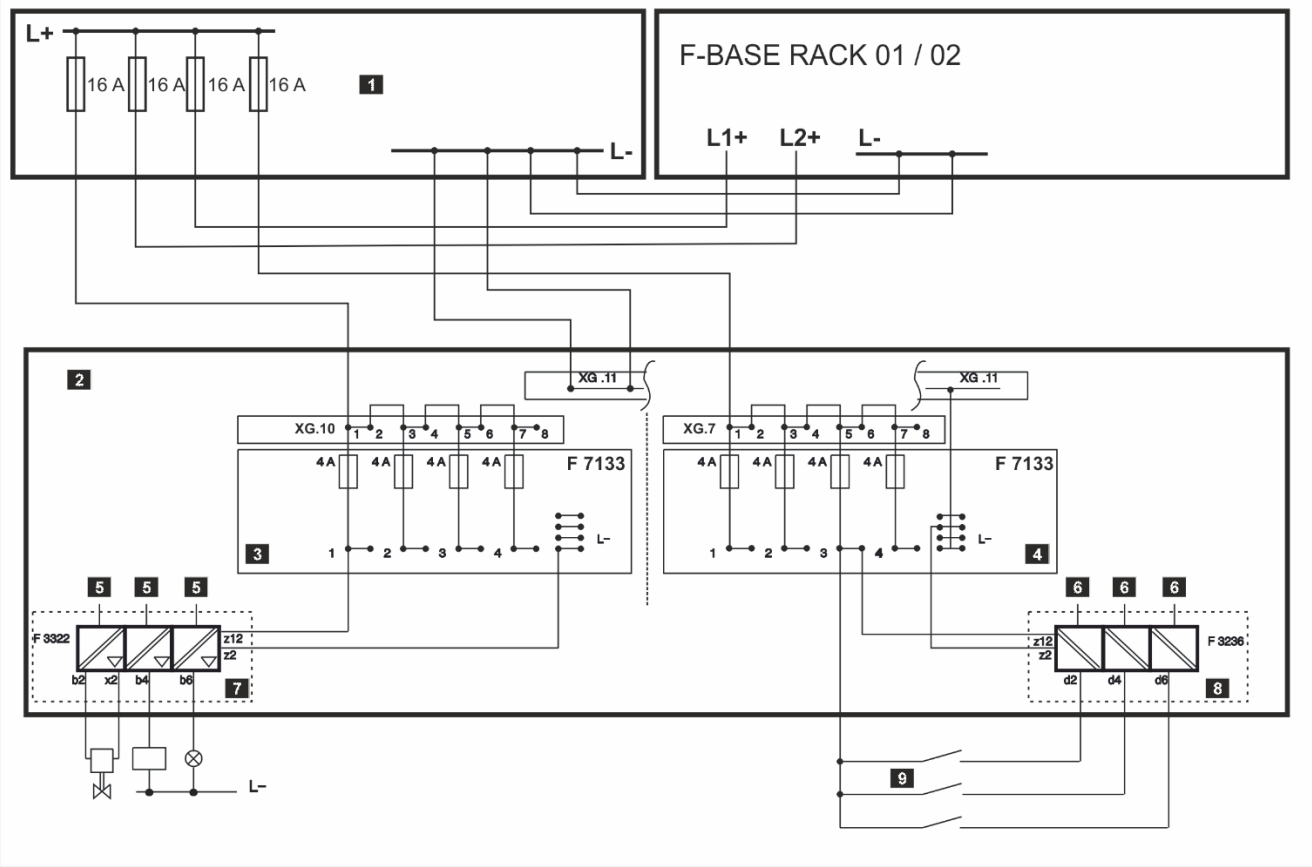
The 24 V power supply is distributed via a fuse and current distribution module connected to the base racks and extension racks.

Each extension rack may be equipped with a maximum of 4 F 7133 power distribution modules. For each F 7133, a back-up fuse (16 A) must be used in the fuse and power distribution module.

Each I/O module in the extension rack is secured by one fuse of the F 7133 power distribution module. Each F 7133 protects 4 slots with 4 A per slot. The assignment of the power distribution modules to the slots of the I/O modules is as follows:

F 7133 power distribution module	Supplies the I/O modules in
Slot 18	Slot 1…4
Slot 19	Slot 5…8
Slot 20	Slot 9…12
Slot 21	Slot 13…16

Table 15: Assignment of F 7133 Power Distribution Modules to I/O Module Slots



1 Fuse and power distribution module, see Chapter 10.
2 Extension rack (F-BASE RACK 11)
3 F 7133 power distribution module, slot 18
4 F 7133 power distribution module, slot 21
5 Output signals
6 Input signals
7 Output module in slot 1 (example)
8 Input module in slot 15 (example)
9 Transmitter 1…3

Figure 27: 24 VDC Distribution for HIQuad X

The I/O modules are either supplied via the front cable plug or via the backplane PCB. The XG.11 potential distributor is connected to the L- of the fuse and power distribution module. All F 7133 power distribution modules are internally connected to the L- of the potential distributor.

The L- is connected to the I/O modules through the front panel of the power distribution module via the cable plugs.

In Figure 27, the power supply of the transmitter circuits is tapped at the front of the F 7133 power distribution module. The transmitters are protected by the same fuse as the input module 8.

4.3.7.1 5 V Distribution for HIQuad X

To generate 5 V power supply, a base rack can be equipped with up to 5 (H41X: 2) F-PWR 01 power supply units that are connected in parallel. The 5 V power supply is distributed to each slot via the backplane PCB. The 5 V power supply is monitored by the power supply units and its status is transmitted to the processor modules. In the user program, system variables can be used to evaluate the status of the power supply units.

4.3.7.2 5 VDC Distribution for H51X

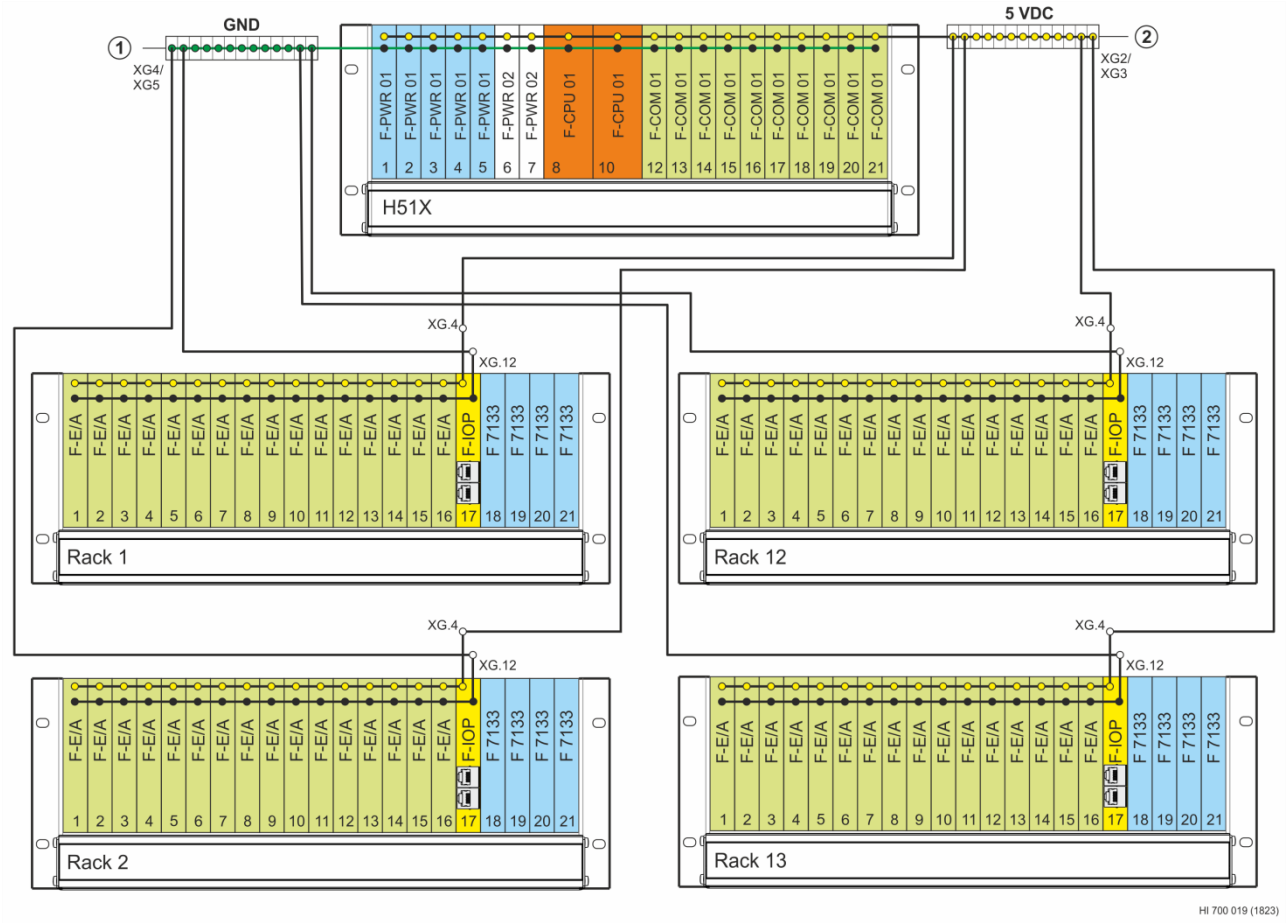
26 connection points can be used to distribute the 5 V power supply through terminal blocks XG2 and XG3 for 5 V, or XG4 and XG5 for GND. The supply voltage is distributed in a star configuration, see Figure 25. The resistance of a 5 V supply line with a maximum length between H51X base rack and extension rack of 12 m must be ≤ 40 mΩ. If cables longer than 3 m are used, HIMA recommends shielding the cables to protect them against transient interference (LIY-CY), and applying the shield at both sides as flat as possible.

To connect cables with a cross-section larger than 2.5 mm², pin terminals with a pin diameter < 2 mm or other suitable transfer terminals can be used.

The I/O processing modules (F-IOP 01) monitor the 5 V power supply of the racks on which they are installed. If the minimum voltage is underrun, I/O processing modules switch off the I/O level of their rack.

HIMA uses yellow wires for 5 V and green wires for GND. If the H51X system is distributed among several control cabinets, separate power supply units may be necessary to supply 5 V to the control cabinets without base rack, see Chapter 4.3.8 for details.

The wires on the extension racks are connected to the flat connectors XG.4 (5 V) and XG.12 (GND), and the shield to the PE connector. The voltage is distributed to the I/O modules via the backplane PCB.



1 GND connectors (XG4 and XG5) on the rack rear side

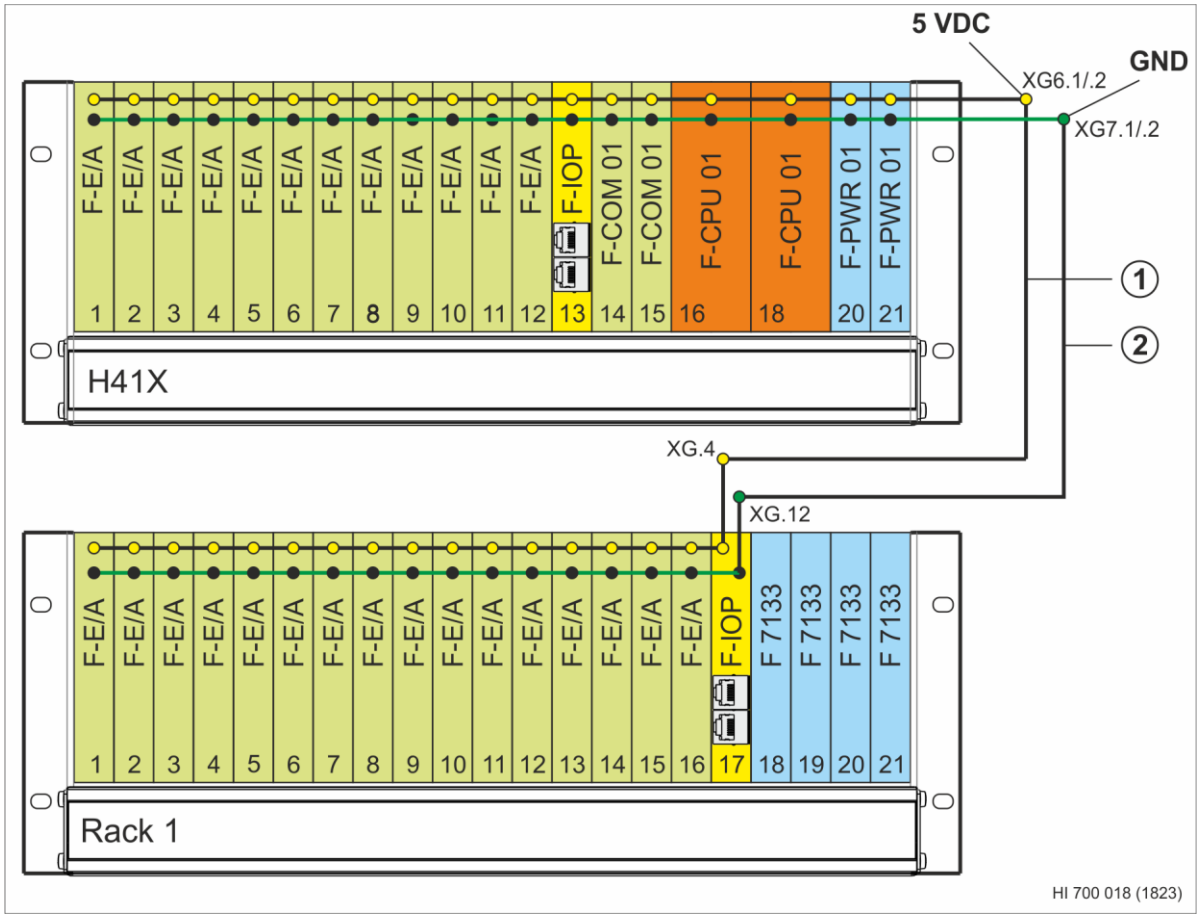
2 5 VDC connectors (XG2 and XG3) on the rack rear side

Figure 28: Extension Rack Connected to a 5 VDC (H51X)

4.3.7.3 5 VDC Distribution for H41X

The 5 V power supply is distributed to the extension rack through terminal blocks XG6 for 5 V and XG7 for GND. The extension rack must be connected to 2 parallel wires (2.5 mm²) for 5 V and GND in a star configuration so that the 5 V power supply is applied to the I/O processing modules at sufficiently high voltage. HIMA uses yellow wires for 5 V and green wires for GND. The wire length within the control cabinet is limited to 3 m. If the H41X system is distributed among two control cabinets, the 5 V power supply must be provided in the control cabinet without base rack by a separate power supply unit, see Chapter 4.3.8 for details.

The wires on the extension rack are connected to the flat connectors XG.4 (5 V) and XG.12 (GND). The voltage is distributed to the I/O modules via the backplane PCB.



1 5 VDC connector XG6.1.2 (base rack), XG.4 (extension rack).

2 GND connector XG7.1.2 (base rack), XG.12 (extension rack).

Figure 29: Extension Rack Connected to a 5 VDC (H41X)

When designing the 5 V voltage supply, the current consumption of all I/O modules and the modules in the base rack must be taken into account. For details on the power consumption of the individual modules, refer to the module-specific manuals.

For HIQuad H51X:

Number of F-PWR 01 power supply units	Maximum permissible current consumption	Availability design (with a failed power supply unit tolerated!)
1	10 A	---
2	20 A	10 A
3	30 A	20 A
4	40 A	30 A
5	40 A	40 A

Table 16: Allowed Power Consumption in Relation to the Number of Power Supply Units

For HIQuad H41X:

Number of F-PWR 01 power supply units	Maximum permissible current consumption	Availability design (with a failed power supply unit tolerated!)
1	10 A	---
2	10 A	10 A

Table 17: Allowed Power Consumption in Relation to the Number of Power Supply Units

4.3.8 5 VDC Additional Power Supply (H51X)

The 5 VDC power supply can be extended by a H51X additional power supply consisting of the B 9361 set and at least an F 7126 power supply unit.

4.4 System Bus

The HIQuad X system is based on the redundant system buses A and B. Each system bus is controlled and monitored by one processor module located in the base rack. For redundant operation, the system must be operated with two processor modules. In redundant operation, communication runs on both system buses simultaneously. If only one processor module is inserted in the base rack, the system runs in mono operation with only one system bus.

Redundant operation ensures that, if one processor module fails, communication is maintained by the redundant processor module via one system bus. To ensure redundant operation again, the defective processor module must be replaced immediately.

It is not allowed to interconnect the system buses of several HIQuad X systems!

No active elements such as switches may be connected to the system bus.

NOTICE

System malfunction possible!

Using system bus connectors XD1...XD4 on the back of the backplane PCB as normal Ethernet connections may cause the system to malfunction.

- **Only use the system bus connectors XD1...XD4 to connect to the I/O processing modules (F-IOP 01).**
- **Do not interconnect or cross system bus A and system bus B.**

The system buses connect the I/O level to the processor modules via the I/O processing modules (F-IOP 01). To do so, the RJ-45 interfaces on the rear side of the base racks must be connected to the I/O processing modules, see Chapter 3.2. The maximum length of the patch cable between two system bus subscribers is 50 m. The cable diameter must be selected in relation to the cable length.

To perform the connection, use patch cables with the following characteristics:

- At least Cat. 5e (in accordance with IEEE 802.3) for 1 Gbit/s, for industrial applications.
- Industrial RJ-45 connectors on both sides.
- The cable shielding must comply with at least Class D in accordance with ISO/IEC 11801.
- Autocrossover allows the use of both crossover and straight through cables.

Suitable patch cables (Cat. 5e) with industrial connector are available from HIMA in standard lengths.

NOTICE

Communication interference possible!

Use patch cables compliant with industrial standard Cat. 5e or better!

In harsh environments (e.g., subject to temperature changes, electromagnetic interference), low-quality patch cables may cause communication to fail.

The maximum system bus latency can be set to System Defaults or 100 µs using the *Maximum System Bus Latency [µs]* system parameter located in the resource properties. When the Maximum System Bus Latency [µs] is set to System Defaults, the maximum system bus latency is determined by the system. For the 100 µs setting, the maximum system bus latency is set to this value!

For system bus connections running within a control cabinet, the minimum cross-section of patch cables must be 0.2 mm².

For system bus connections running outside a control cabinet, the minimum cross-section of patch cables must be 0.5 mm². If necessary, installation cables with rigid cores must be used instead of patch cables with flexible cores.

4.5 I/O Bus

All I/O modules are connected to the I/O processing module via the I/O bus. The I/O processing module in the H41X base rack (slot 13) and in the extension rack (slot 17) connect the I/O bus to the system buses.

4.6 I/O Watchdog (WD)

A second independent shutdown option is required in safety-related systems. This is ensured by an I/O watchdog signal (24 V). The I/O watchdog is controlled, monitored, and applied to the output modules by the I/O processing modules. The output modules only operate when the watchdog signal is present (high level). If the I/O watchdog signal is switched off, the output modules safely enter the de-energized state.

4.7 Modules

The HIQuad X system is a modular system that can be equipped with various modules. The following modules are available for the system:

- F-CPU 01 processor module
- F-IOP 01 I/O processing module
- F-COM 01 communication module
- I/O modules, see Chapter 4.11
- F-PWR 01 power supply unit (24/5 V)
- F-PWR 02 buffer module

4.8 F-CPU 01 Processor Module

The CPU operating system controls the user programs running in a processor module.

4.8.1 Operating System

Tasks:

- Controlling the cyclic run of the user programs.
- Performing the self-tests of the module.
- Controlling safety-related communication via safe**ethernet.**
- Managing the processor modules' redundancy (synchronization).

4.8.1.1 General Cycle Sequence

Phases:

1. Reading of the input data.
2. Processing of the user program.
3. Writing of the output data.
4. Other activities, e.g., reload processing.

4.8.1.2 Operating System States

States that can be recognized by the user:

- LOCKED
- STOP/VALID CONFIGURATION
- STOP/INVALID CONFIGURATION
- STOP/LOADING OS
- RUN
- RUN/UP STOP

Use the LEDs on the module to recognize the operating state. All LEDs must be taken into account, see the module-specific manuals.
SILworX displays the operating states in the online view.

State	Description	The state is entered:
LOCKED	The processor module is reset to the factory settings (SRS, network settings, etc.).	Connecting the supply voltage to the processor module while the mode switch is set to Init.
STOP/VALID CONFIGURATION	Processor module stopped: A valid configuration is available in the memory.	Stopping the processor module using SILworX.
		Applying the supply voltage ▪ Autostart is disabled in the project configuration or ▪ Mode switch is set to Stop and the processor module starts by itself.
		A fault occurred.
STOP/INVALID CONFIGURATION	Processor module stopped: No valid configuration is available in the memory.	Loading with error.
STOP/LOADING OS	Processor module stopped: The operating system is loaded in the non-volatile memory.	Loading the operating system using SILworX.
RUN	The user program is running.	From the STOP/VALID CONFIGURATION state: SILworX command.
		Applying the supply voltage, the following conditions must be met: ▪ A valid project configuration is loaded. ▪ Autostart is enabled in the project configuration. ▪ The mode switch is not set to Init. ▪ The mode switch is set to Run if the processor module starts by itself.
RUN/UP STOP	The user program is not running. This state is used for testing the inputs/outputs and communication.	From the STOP/VALID CONFIGURATION state: SILworX command SILworX.

Table 18 provides an overview of the operating system states and indicates the conditions for entering them.

State	Description	The state is entered:
LOCKED	The processor module is reset to the factory settings (SRS, network settings, etc.).	Connecting the supply voltage to the processor module while the mode switch is set to Init.
STOP/VALID CONFIGURATION	Processor module stopped: A valid configuration is available in the memory.	Stopping the processor module using SILworX.
		Applying the supply voltage ▪ Autostart is disabled in the project configuration or ▪ Mode switch is set to Stop and the processor module starts by itself.
		A fault occurred.
STOP/INVALID CONFIGURATION	Processor module stopped: No valid configuration is available in the memory.	Loading with error.
STOP/LOADING OS	Processor module stopped: The operating system is loaded in the non-volatile memory.	Loading the operating system using SILworX.
RUN	The user program is running.	From the STOP/VALID CONFIGURATION state: SILworX command.
		Applying the supply voltage, the following conditions must be met: ▪ A valid project configuration is loaded. ▪ Autostart is enabled in the project configuration. ▪ The mode switch is not set to Init. ▪ The mode switch is set to Run if the processor module starts by itself.
RUN/UP STOP	The user program is not running. This state is used for testing the inputs/outputs and communication.	From the STOP/VALID CONFIGURATION state: SILworX command SILworX.

Table 18: Operating System States, States Entered

Table 19 specifies how the user may intervene during the corresponding states.

State	Possible user interventions
LOCKED	▪ Changing the factory settings. ▪ Using a PADT command to stop (STOP state). ▪ Using a PADT command to start (RUN state).
STOP/VALID CONFIGURATION	▪ Loading the user program. ▪ Starting the user program. ▪ Loading the operating system. ▪ Taking preliminary actions for forcing variables.
STOP/INVALID CONFIGURATION	▪ Loading the user program. ▪ Loading the operating system.
STOP/LOADING OS	None. Once the loading process is completed, the processor module stops (STOP state).
RUN	▪ Stopping the user program. ▪ Forcing variables. ▪ Performing the test.
RUN/UP STOP	▪ Using a PADT command to stop (STOP state).

Table 19: Operating System States, User Interventions

i The cycle time increases by the number of modules used in the system. This applies irrespective of whether or not the modules are included in the configuration.

- **Connecting additional extension racks with several modules during operation can cause the watchdog time to be exceeded!**

4.8.2 Behavior in the Event of Faults

If faults occur, the processor module enters the error stop state and tries to restart. It performs a complete self-test which can also cause another error stop.

If a fault is still present, the module restarts with reduced functionality to prevent a reboot loop.

Once the processor module has properly run for one minute, the next error stop to occur is considered the first *error stop* attempting a restart.

i Use the PADT for troubleshooting and removing the cause of the fault, e.g., by loading a new application.

4.9 F-IOP 01 I/O Processing Module

The I/O processing module manages the I/O bus of the H41X base rack and that of the extension racks. The I/O bus is used to exchange process data between I/O modules and the I/O processing module. The module's tasks include exchanging data with the processor modules and providing the watchdog signal to the output modules via system bus A and system bus B.

4.10 F-COM 01 Communication Module

The communication module is equipped with 2 Ethernet interfaces and 1 fieldbus interface allowing the HIQuad X system to communicate with external systems. The module is approved for use in the safety-related HIQuad X system and can be employed to transport safety-related protocols.

4.11 I/O Modules

The following table shows the I/O modules that can be used for HIQuad X:

Module	Cable plug	Channels	SIL	Type	Data sheet HI number
F 3221	Z 7116 / 3221	16	---	DI	HI 803 174 E
F 3224A	Z 7114 / 3224	4	---	DI; (Ex)i	HI 803 175 E
F 3236	Z 7116 / 3236	16	3	DI	HI 803 176 E
F 3237	Z 7108 / 3237	8	3	DI	HI 803 177 E
F 3238	Z 7008 / 3238	8	3	DI; (Ex)i	HI 803 178 E
F 3240	Z 7130 / 3240	16	3	DI 110 VDC	HI 803 179 E
F 3248	Z 7130 / 3248	16	3	DI 48 VDC	HI 803 180 E
F 3322	Z 7136 / 3322	16	---	DO 0.5 A	HI 803 181 E
F 3325	Z 7025 / 3325	6	---	Supply module	HI 803 182 E
F 3330	Z 7138 / 3330	8	3	DO 0,5 A	HI 803 183 E
F 3331	Z 7138 / 3331	8	3	DO 0.5 A	HI 803 184 E
F 3333	Z 7134 / 3333	4	3	DO 2 A	HI 803 185 E
F 3334	Z 7134 / 3334	4	3	DO 2 A	HI 803 186 E
F 3335	Z 7035 / 3335	4	3	DO; (Ex)i	HI 803 187 E
F 3349	Z 7150 / 3349	8	3	DO 0.5 A	HI 803 188 E
F 3422	Z 7139 / 3422	8	---	Relay 60 VDC	HI 803 189 E
F 3430	Z 7149 / 3430	4	3	Relay 110 VDC	HI 803 190 E
F 5220	Z 7152 / 5220	2	3	Counter	HI 803 191 E
F 6215	Z 7127 / 6215	8	---	AI	HI 803 192 E
F 6217	Z 7127 / 6217	8	3	AI	HI 803 193 E
F 6220	Z 7062 / 6220	8	3	Thermocouple; (Ex)i	HI 803 194 E
F 6221	Z 7063 / 6221	8	3	AI; (Ex)i	HI 803 195 E
F 6705	Z 7126 / 6705	2	3	AO	HI 803 196 E
F 6707	Z 7126 / 6706	2	---	AO	HI 803 197 E

Table 20: Possible I/O Modules to Be Used in HIQuad X

4.11.1 Scope of Application of the I/O Modules

Refer to the safety manual (HI 803 209 E) for more information on the standards used to certify the I/O modules.

i For the scope of application of the I/O modules, observe the revisions, see the modernization manual (HI 803 235 E).

4.11.2 Mounting Position

The I/O modules must be mounted vertically. The vertical mounting position automatically results from the horizontal position of the rack within a control cabinet.

4.12 Noise Blanking

This chapter describes how noise blanking of I/O modules operates in the HIQuad X system.

4.12.1 Effects of Noise Blanking

Noise blanking suppresses transient interference to increase the system availability. It ensures that the system triggers a safety-related response to existing interferences within the configured time.

Noise blanking can be activated for I/O modules. For details, refer to the SILworX Hardware Editor and the module-specific manuals.

If an interference is blanked out, the system automatically processes the last valid input and output values instead of the currently disturbed values. The time in which noise can be blanked out is limited by the safety time, watchdog time and the cycle time.

The maximum noise blanking time can be calculated using the following equation:

Maximum noise blanking time = safety time - (2 x watchdog time)

The greater the noise blanking time value, the longer the interference can be blanked out. Since an interference can be present for up to one cycle before it is detected while reading in the values, the minimum noise blanking time can be determined by subtracting a cycle from the maximum noise blanking time value.

Minimum noise blanking time = maximum noise blanking time - cycle time

Noise blanking is effective if the cycle time value is less than the noise blanking time.

4.12.2 Configuring Noise Blanking

To blank out as many cycles as possible, the safety time must be set as large as possible taking the process safety time into account. At the same time, the value set for the watchdog time should be as low as possible, but sufficiently large to allow reload and synchronization of an additional processor module. Refer to the safety manual (HI 803 209 E) for further details on the various time parameters and their application.

Configure noise blanking in accordance with the following examples:

Example	1	2	3
Safety Time [ms]	600	2000	1000
Watchdog Time [ms]	200	500	500
Target Cycle Time [ms]	100	200	200
Max. Noise Blanking Time [ms]	200	1000	0
Min. Noise Blanking Time [ms]	100	800	0

1) Default setting in SILworX.

2) No noise blanking is possible in example 3 since the noise blanking time is less than the cycle time.

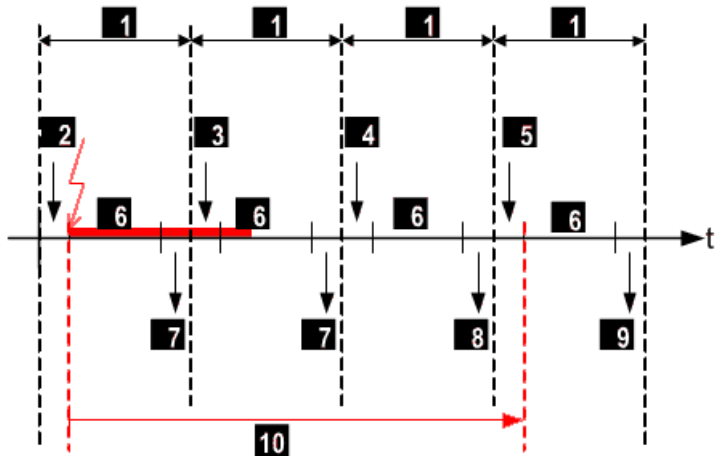
Table 21: Example for Calculating the Minimum and Maximum Noise Blanking Time

4.12.3 Noise Blanking Sequence

The following examples illustrate the sequence of noise blanking:

- A transient interference is blanked out.
- An interference present for longer than the maximum noise blanking time triggers the safe response.

Example 1: Transient interference is successfully blanked out



1	Cycle, duration = watchdog time	6	Processing (in all cycles)
2	Reading in cycle 1	7	Output process in cycle 1 and 2
3	Reading in cycle 2	8	Output process in cycle 3
4	Reading in cycle 3	9	Output process in cycle 4
5	Reading in cycle 4	10	Duration of safety time

Figure 30: Transient Interference

In example 1, valid input values 2 are read within one cycle. For this cycle, the system processes the valid input values, even though an interference occurred directly upon completion of the read-in process. If the interference is still present in the following cycle during the read-in process 3, the module detects the interference and the system decides if noise blanking can be performed at this point in time based on the following rule:

Safety time - elapsed time - (2 x watchdog time) > 0

Elapsed time = Time interval between the moment, in which the last valid values were read in, and the moment, in which the interference was detected.

In this example, noise blanking is possible since the interference is present for less than a cycle (= elapsed time) and two additional cycles (2 x watchdog time) are available for triggering a safe response. For this cycle, the system processes the last valid input values of 2 and no fault response is triggered. The transient interference was successfully blanked out.

If the interference is no longer present in 4, new valid values are read in and processed. If noise blanking is not active, the system immediately triggers the defined fault response during the read-in process 3.